


PAGE3;RESERVE RN65~71 P/L 49.9ohms for ICS951464  
PAGE3;CHANGE R107,R108 from 47.5 ohms TO 0ohm;Need CHECK!!  
PAGE14;CHANGE LCD1;PIN27 TO TP105;RESERVE FOR LIGHT SENSOR  
PAGE14;CHANGE LCD1;PIN24 TO 5V POWER RAIL FOR LED DRIVER BOARD IC ENABLE PIN(HIGH ACTIVE)  
PAGE14;CHANGE F1 TO 4A  
PAGE14;P/U TMDS DDC DAT TO 3D3V S0,ADD R471  
PAGE15;CHANGE RI84,R185,R188 FROM 75ohms TO 150 ohms  
PAGE19;SWAP USB PAIR OF FT AND MINICARD

PAGE27;CHANGE Q11 TO 84.00143.B1K  
PAGE30;CHANGE C389,C390 TO 1uF,X5R  
PAGE30;CHANGE R450,R453 TO 14Kohms  
PAGE30;CHANGE R459,R463 TO 40.2ohms  
PAGE30;CHANGE R458,R462 TO 33ohms  
PAGE31;ADD R472 AND P/H TO 3D3V S0 FOR CAPA\_INT#  
PAGE31;CHANGE R347 TO 4.7Kohms(E51\_TxD P/L)

- PAGE31
- 1.KBC Beep change from A\_PWM0(32) to GPIO56(31)
  - 2.Power LED change from GPIO32(65) to A\_PWM0(32)
  - 3.e-Button LED change from GPIO43(20) to A\_PWM1(118)

LAYOUT

		<b>Wistron Incorporated</b> 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title <b>Change List</b>			
Size A	Document Number <b>Ferrari 7</b>		Rev SA
Date:	Thursday, August 02, 2007	Sheet	1 of 47

# Ferrari 7 Block Diagram

Friday Practice (SA)  
Saturday Practice (SB)  
Qualifying (SC)  
Race (-1)

2006/04/17

Project code:  
PCB P/N :  
REVISION :

**ezDockII/II+**

USB/Express  
Card/MediaBay/1394\*2port  
RJ45/RJ11/PS2\*2/Serial  
Port/Parallel  
Port/CRT/TV/DVI-D/SPDIF/MIC  
in/Line in/Line out/AC Jack

**PCB Layer Stackup**

L1: Component  
L2: GND  
L3: Signal  
L4: VCC  
L5: Signal  
L6: Signal  
L7: GND  
L8: Component

**CPU V\_CORE**  
ISL6264 38/39

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

**SYSTEM DC/DC**  
TPS51124 47

INPUT	OUTPUT
DCBATOUT	ID2V_S0 ID8V_S3

**SYSTEM DC/DC**  
ISL6236 46

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

**SYSTEM LDO**  
TPS51100 48

INPUT	OUTPUT
1D8V_S3	0D9V_S3

**SYSTEM LDO**  
APL5915 48

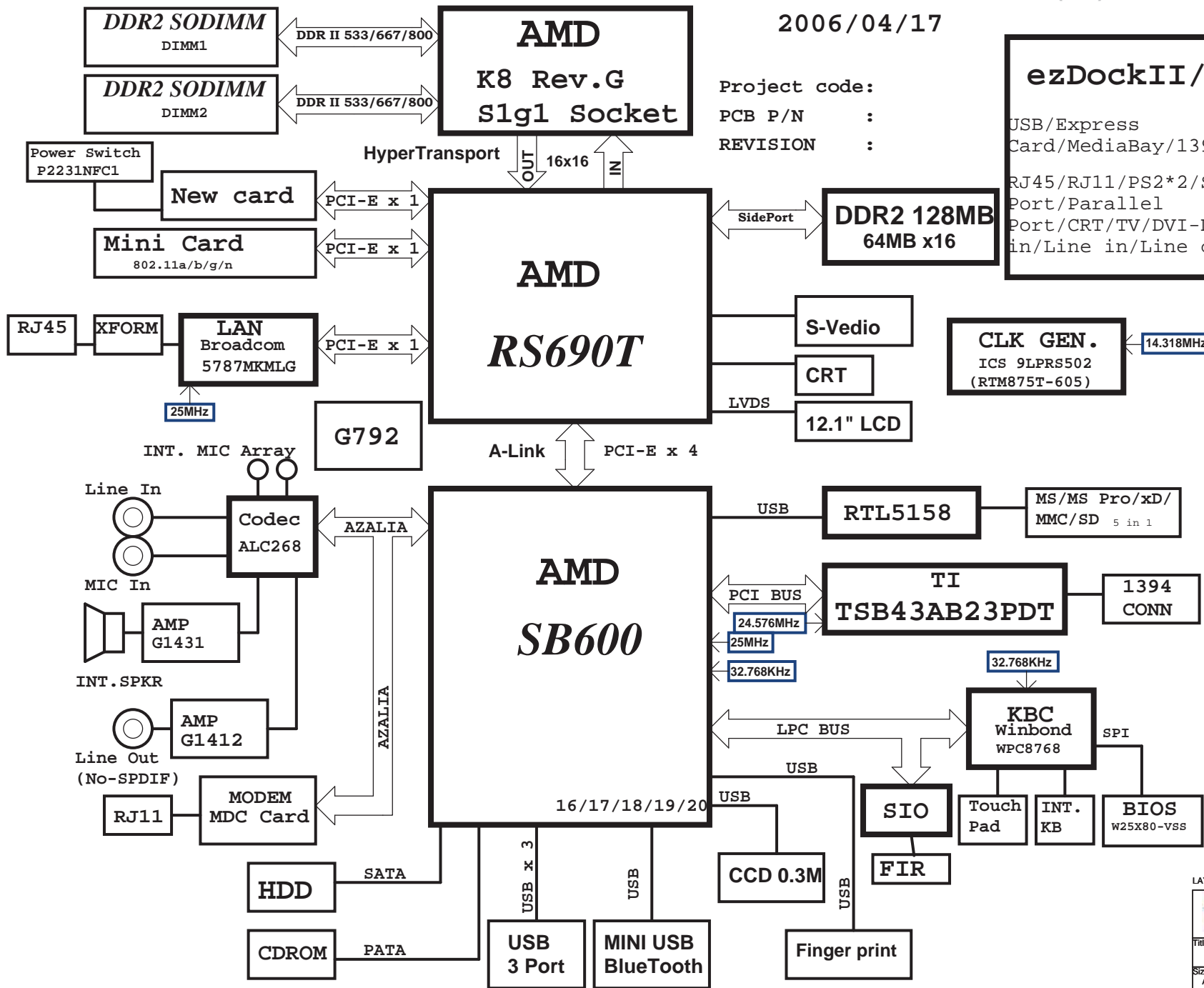
INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	ID2V_S5 2D5V_S0 ID5V_S0

**SYSTEM LDO**  
ISL6236 46

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

**Battery Charger**  
ISL6255 42

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT



**LAYOUT**

**wistron** Wistron Incorporated  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title: **Interactive Circuit Map**

Size: A3 Document Number: **Ferrari 7** Rev: SA

Date: Thursday, August 02, 2007 Sheet: 2 of 47

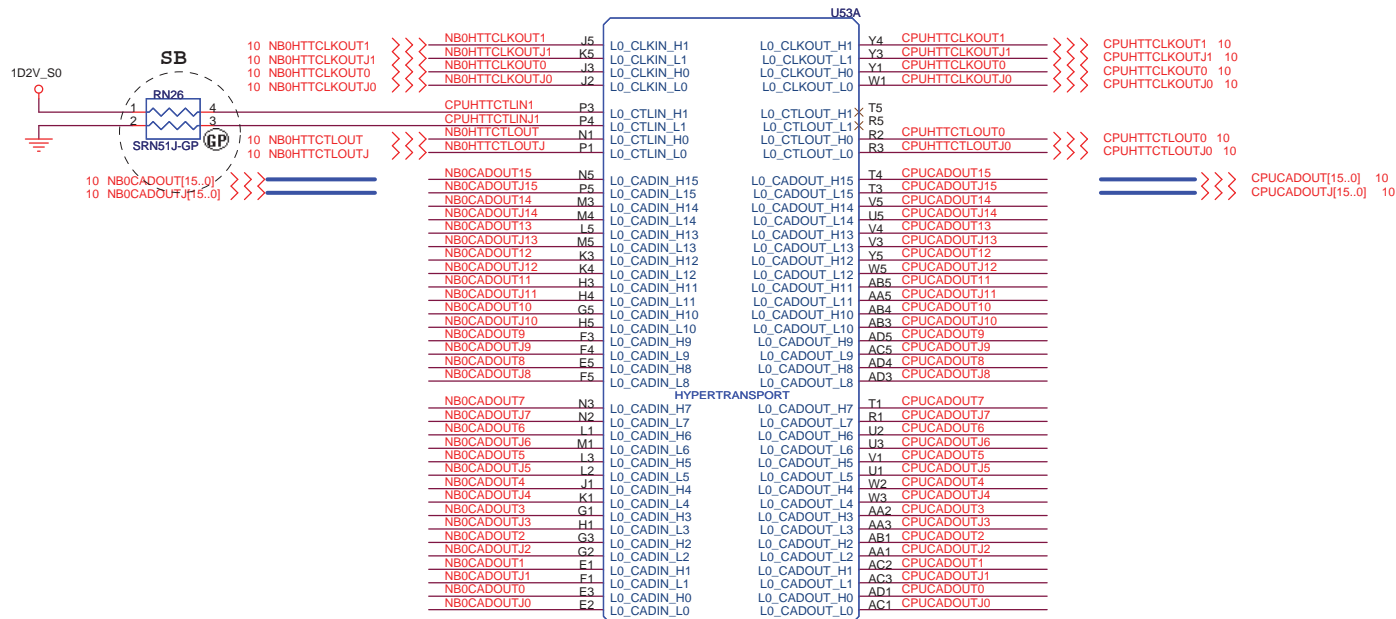
FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation



## LAYOUT

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

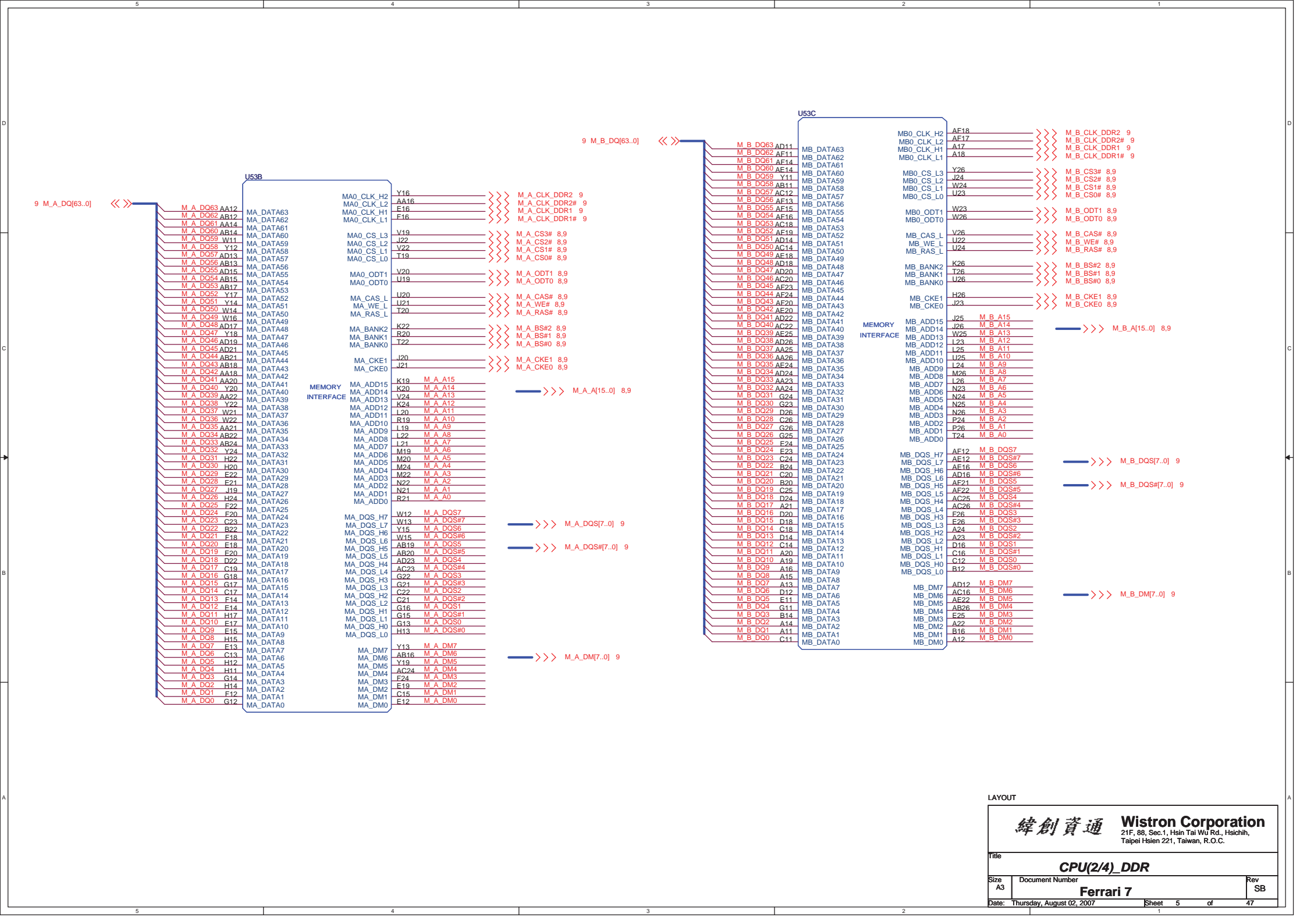
Title			
<b>CLKGEN_ICS951464</b>			
Size A3	Document Number		Rev SB
	<b>Ferrari 7</b>		
Date: Thursday, August 02, 2007	Sheet 3	of	47



62.10055.111

LAYOUT

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
CPU(1/4)_HyperTransport I/F			
Size	Document Number	Rev	
A3		SB	
Date: Thursday, August 02, 2007			
Sheet 4 of 47			



緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichu,

Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU(2/4)\_DDR

Size

Document Number

Rev

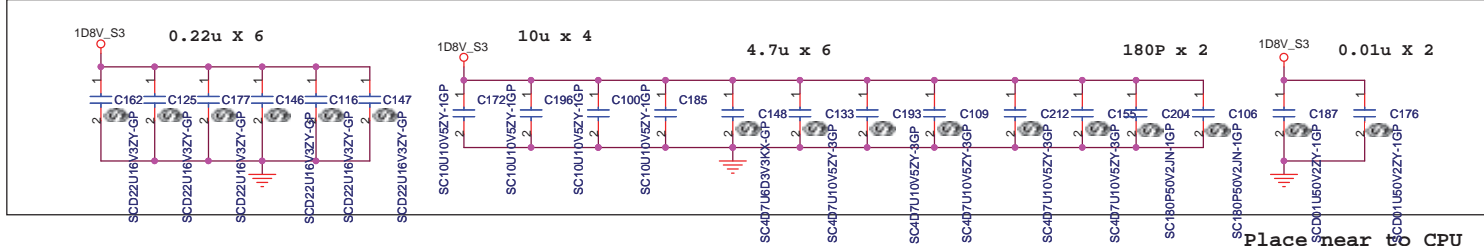
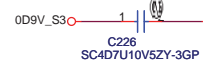
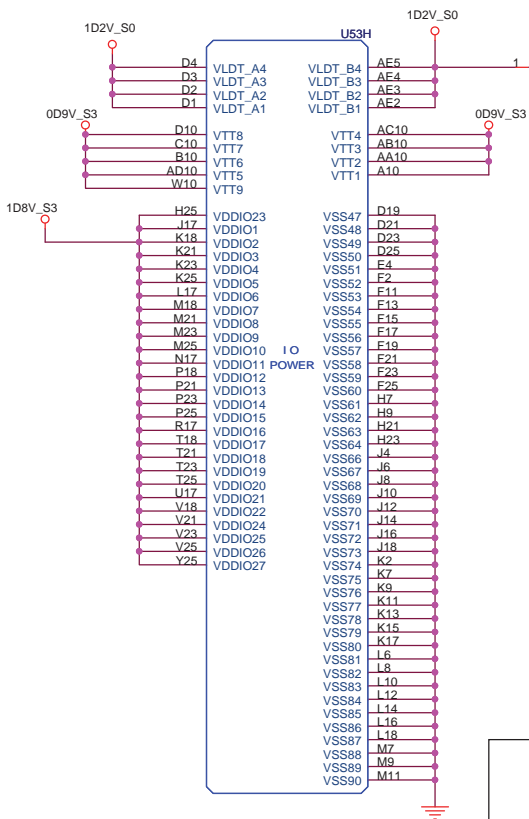
Ferrari 7

SB

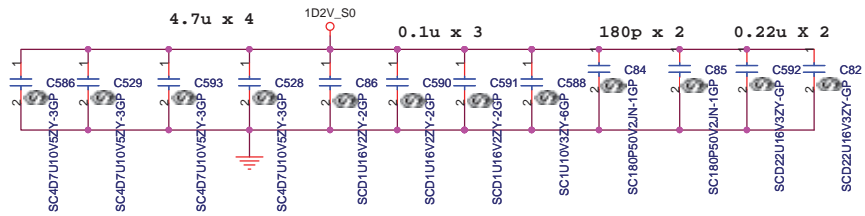
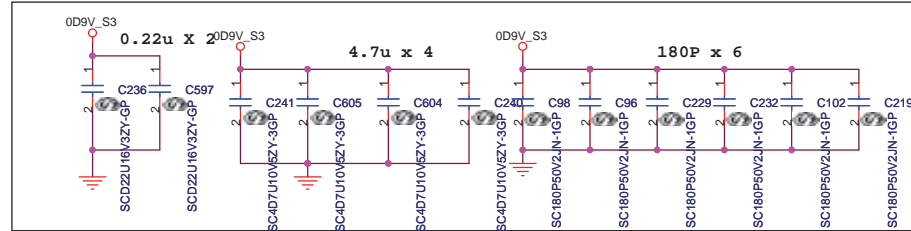
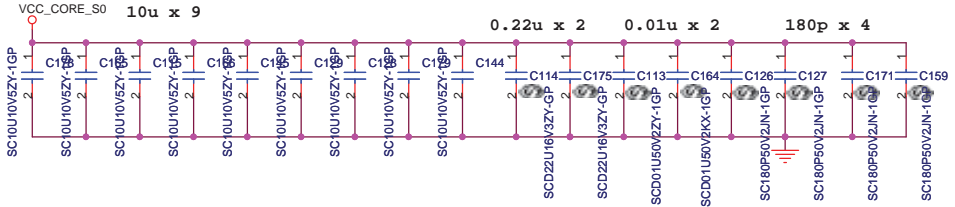
Date: Thursday, August 02, 2007

Sheet 5 of 47





LAYOUT: Place on backside of processor.



LAYOUT

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(4/4)\_Power**

Size A3	Document Number	Rev SB
Date: Thursday, August 02, 2007		Sheet 7 of 47







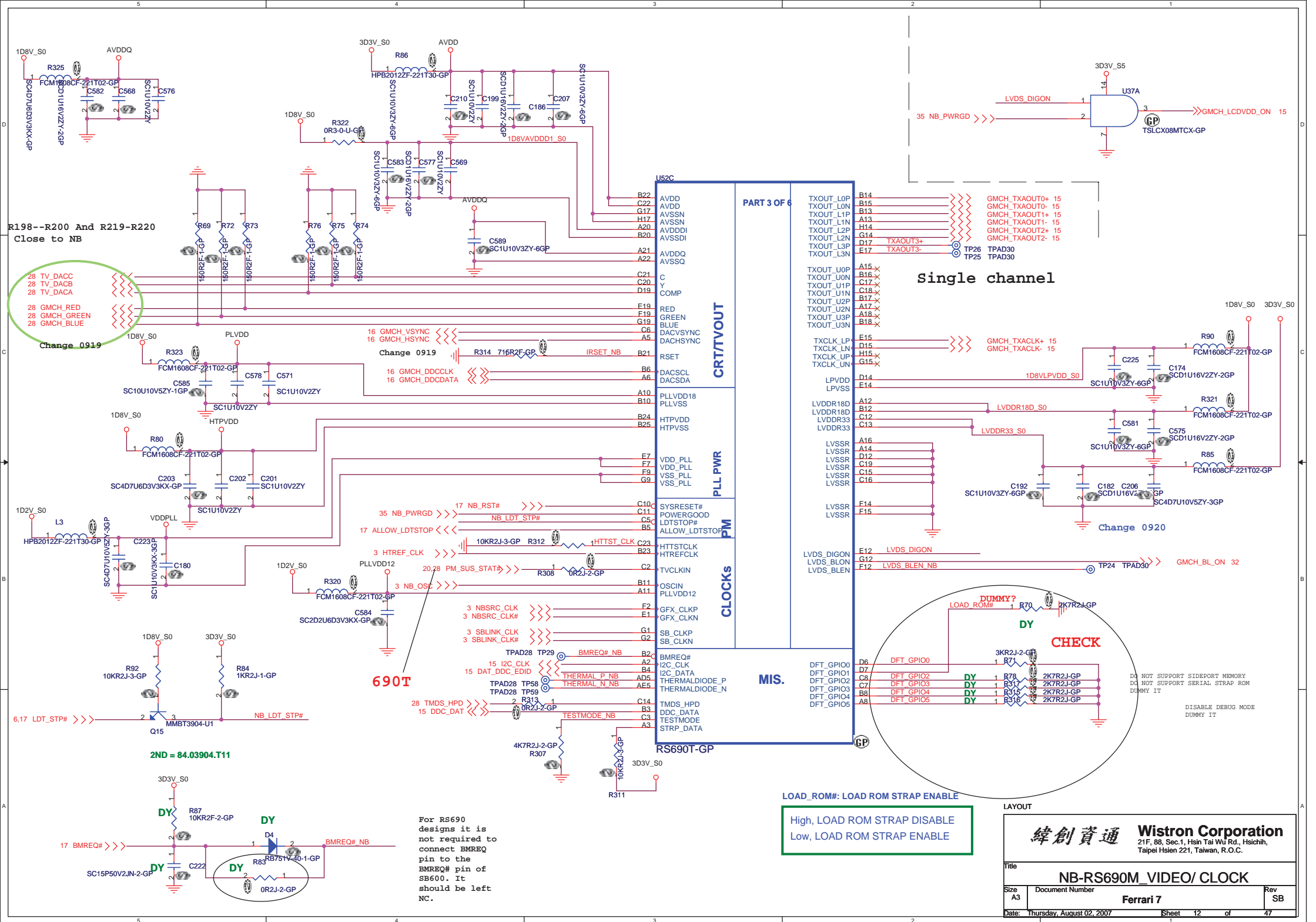


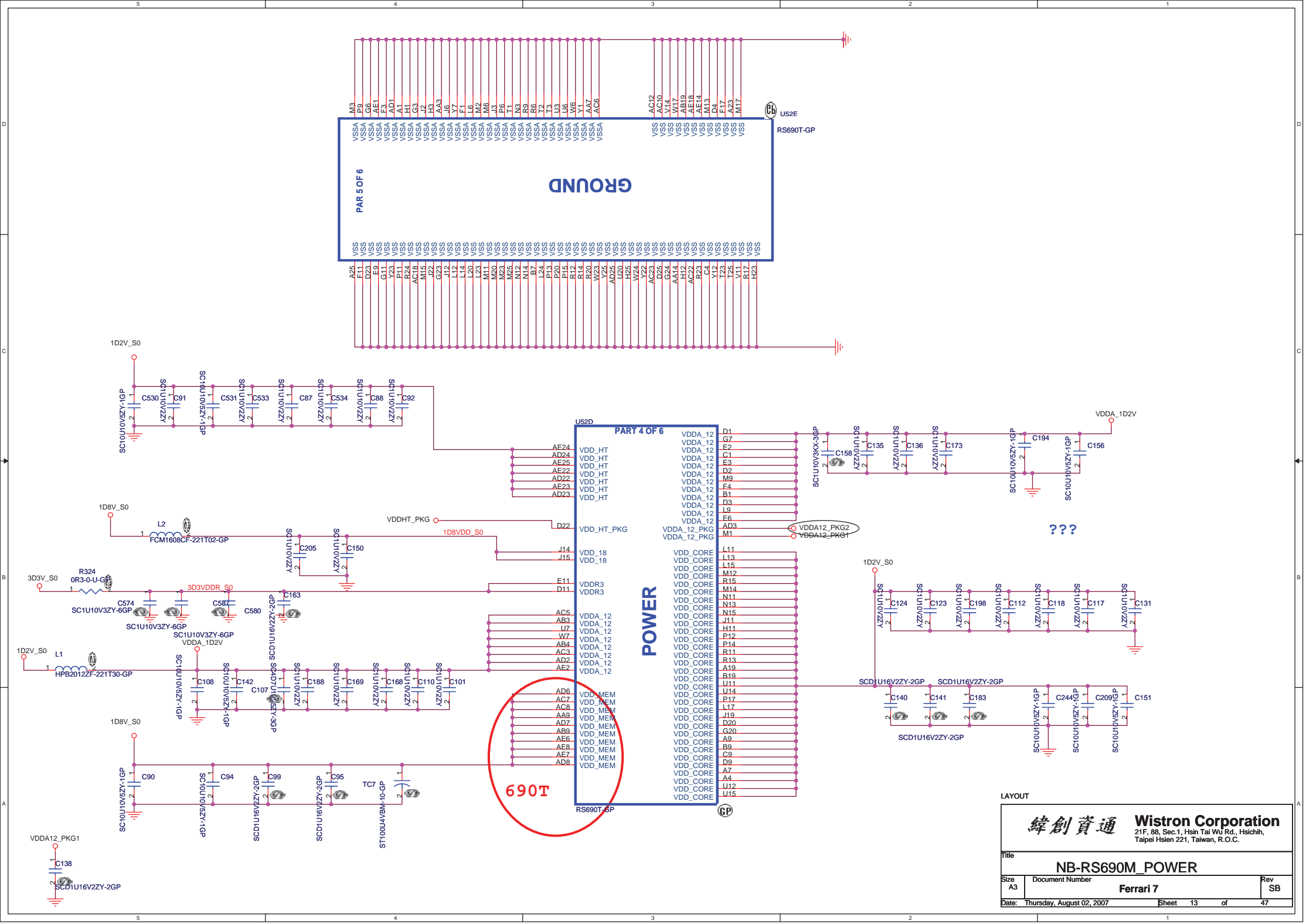
**NB TO CLAW HAMMER**

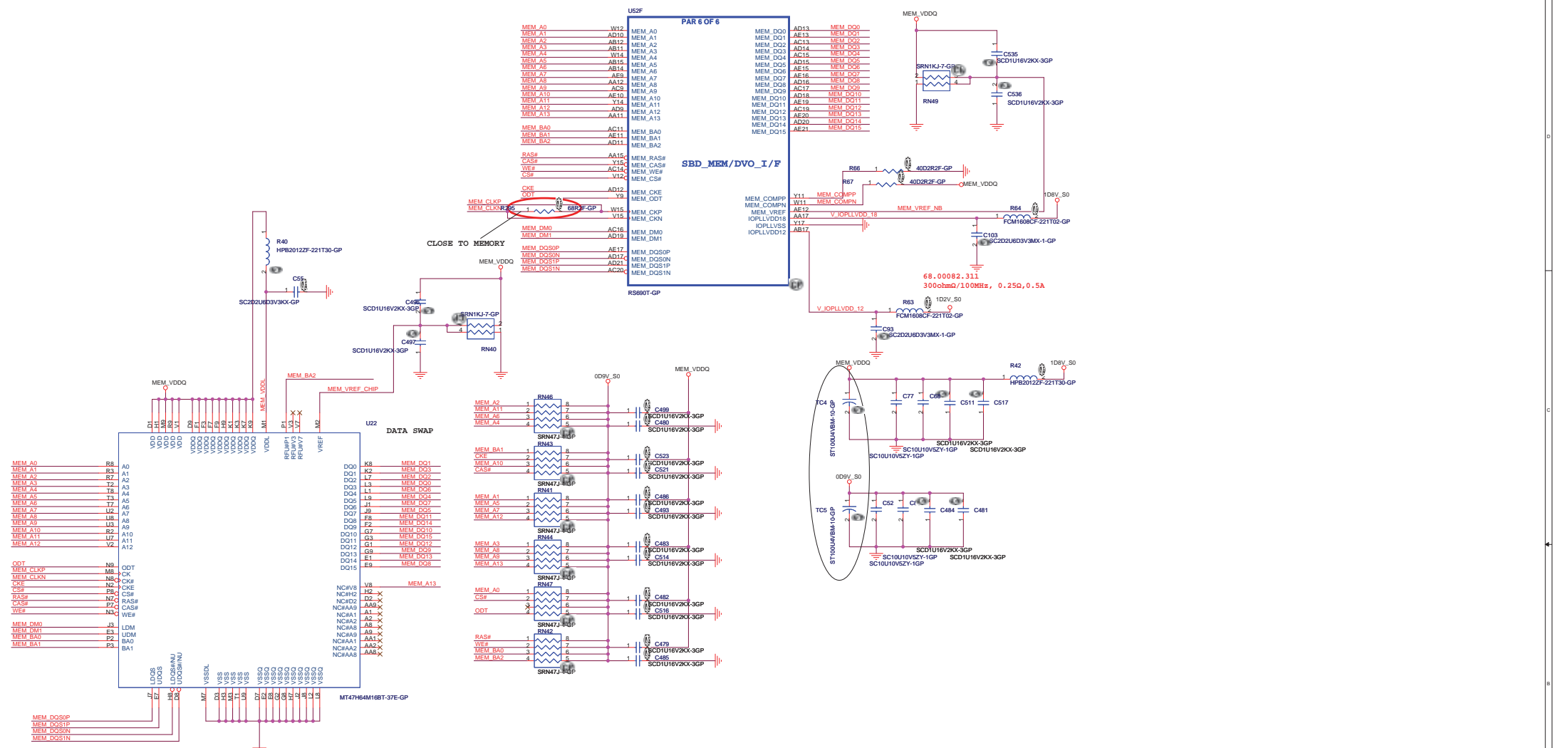


Title			
<b>NB-RS690T HT</b>			
Size A3	Document Number		Rev
	<b>Ferrari 7</b>		<b>SB</b>
Date:	Thursday, August 02, 2007	Sheet 10 of 47	

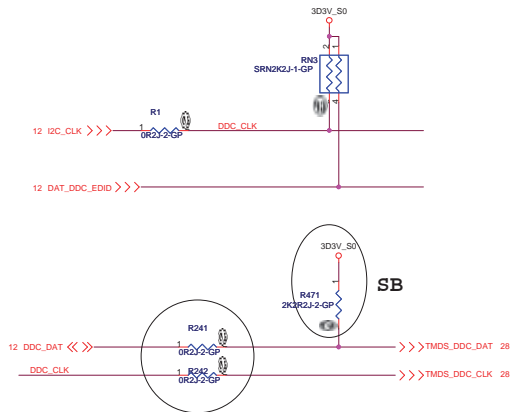








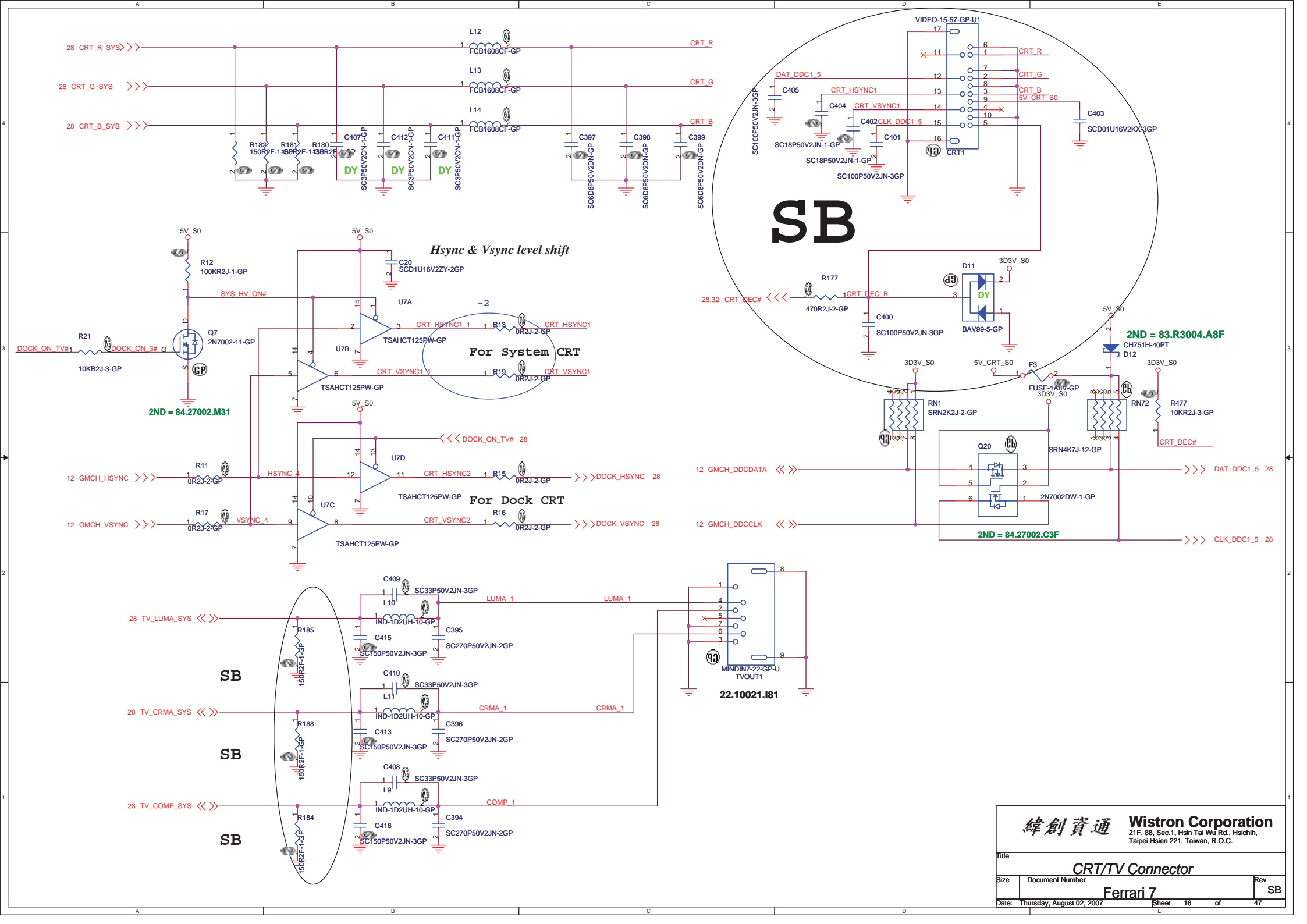
2ND = HYNIX 32M\*16 72.51216.F0U; 72.18512.M0U Qimonda 32M\*16



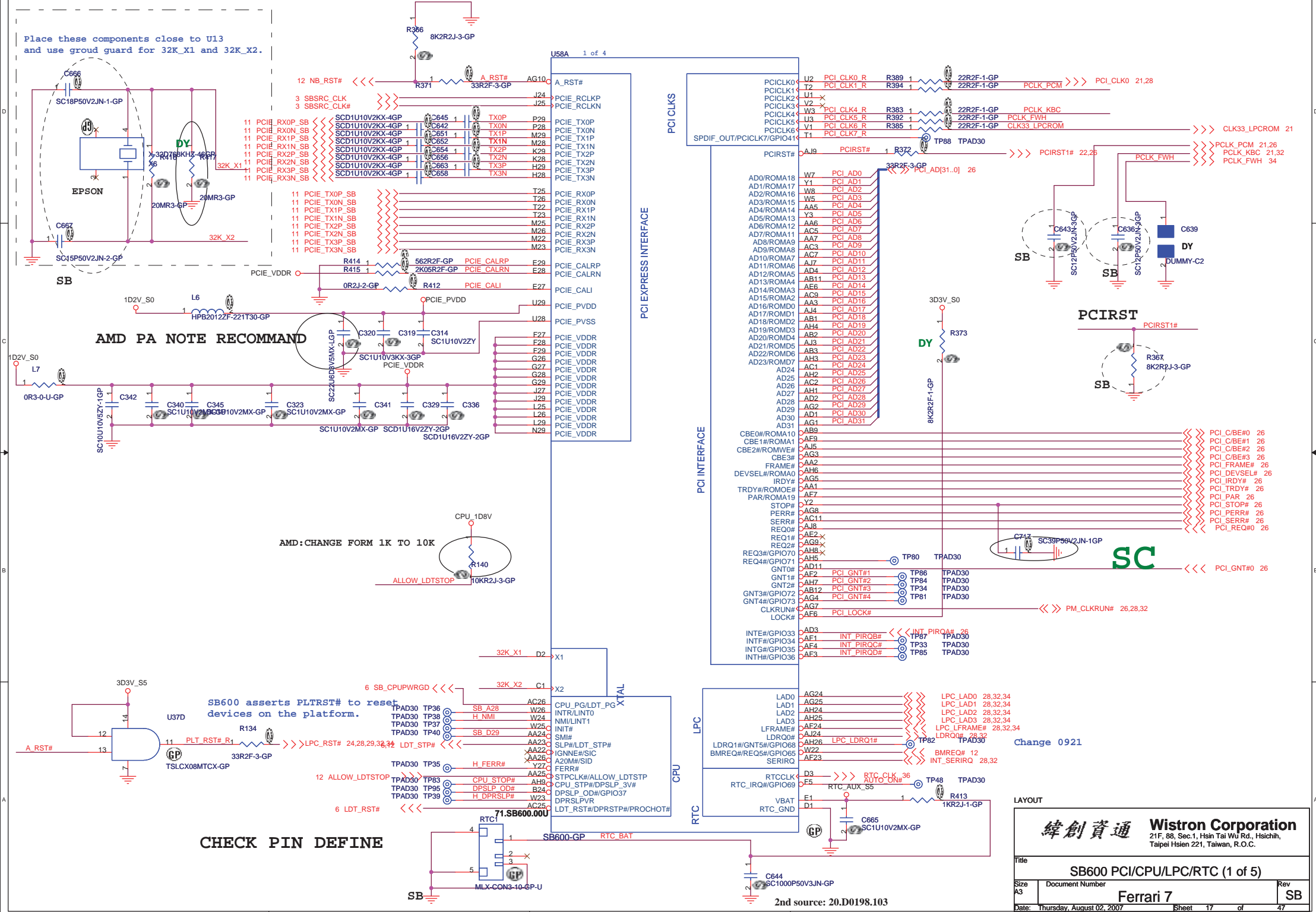
	LVDS	TMS
I2C_CLK	I2C_CLK	I2C_CLK
I2C_DATA	I2C_DATA	
DDC_DATA		DDC_DATA







Place these components close to U13  
and use groud guard for 32K\_X1 and 32K\_X2.



2nd source: 20.D0198.103

PLACE SATA AC DECOUPLING  
CAPS CLOSE TO SB460

GPIO55  
GPIO56  
GPIO54

000Hynix 32M\*16  
010Qimonda 32M\*16  
001Samsung 32M\*16  
011Micron 32M\*16  
100Hynix 64M\*16  
110Qimonda 64M\*16  
101Samsung 64M\*16  
111Micron 64M\*16

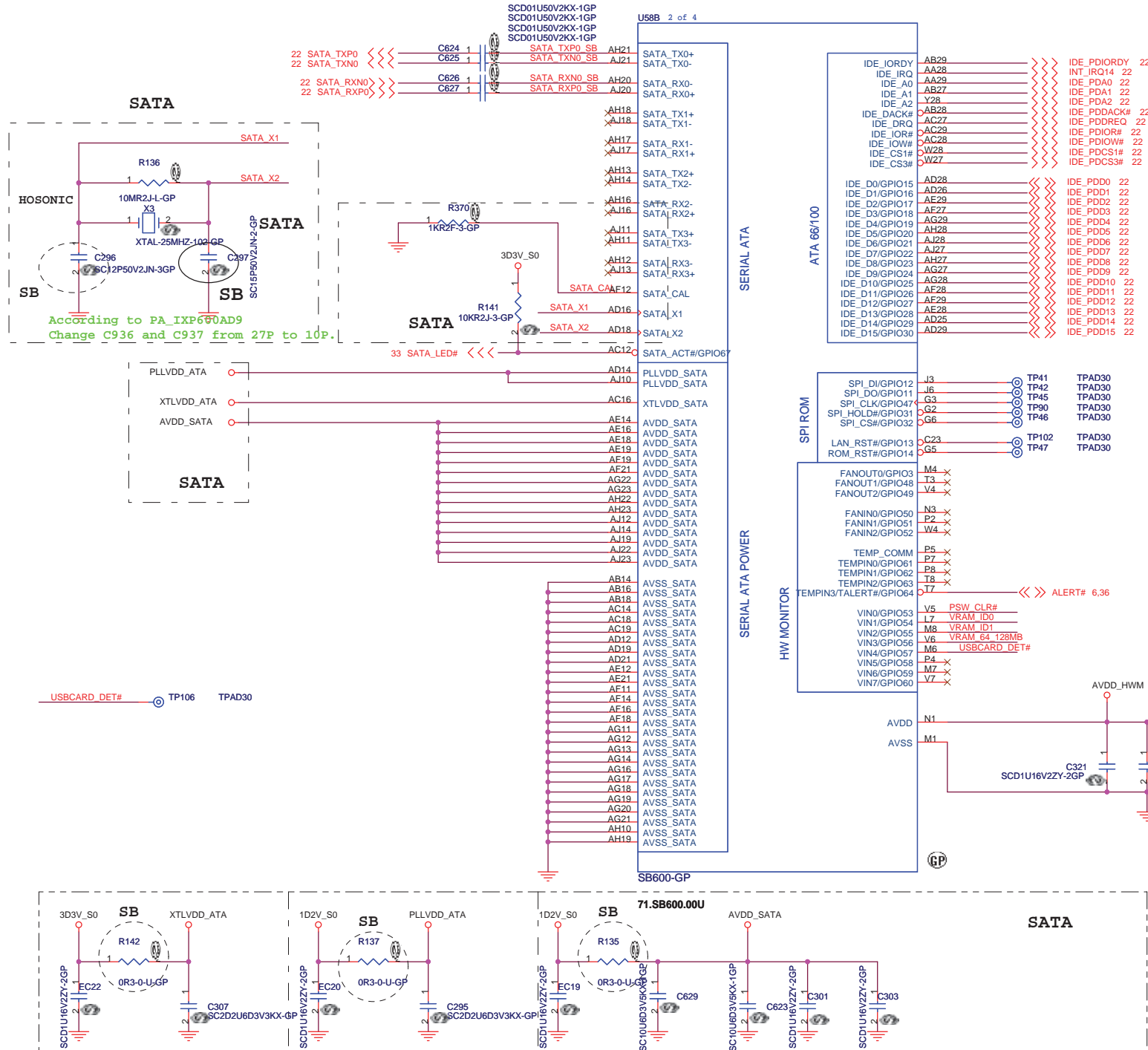
FP DETECT STILL NEED??

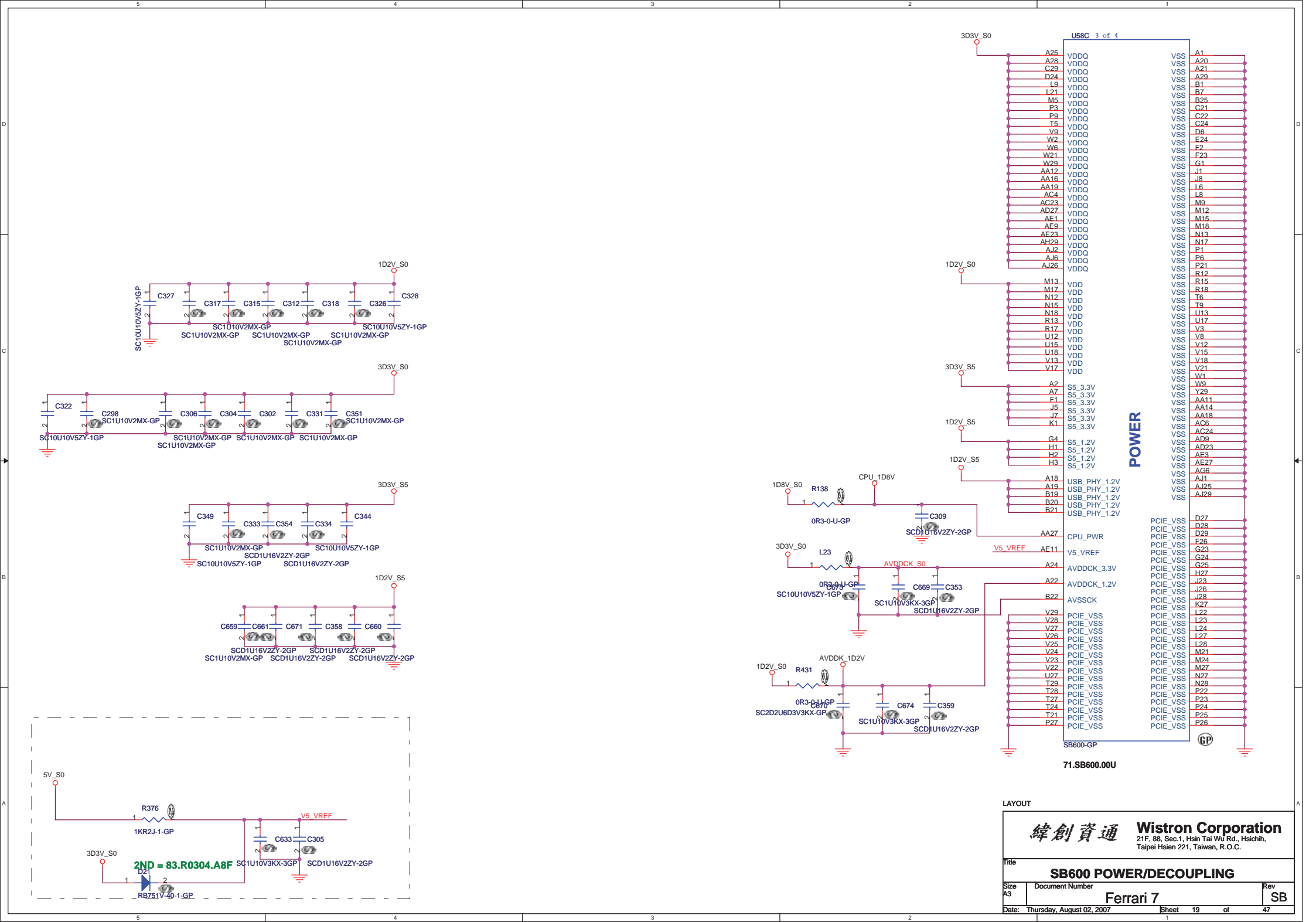
VRAM\_SAMSUNG  
VRAM\_Q  
VRAM\_H\_Q  
VRAM\_H\_M\_S

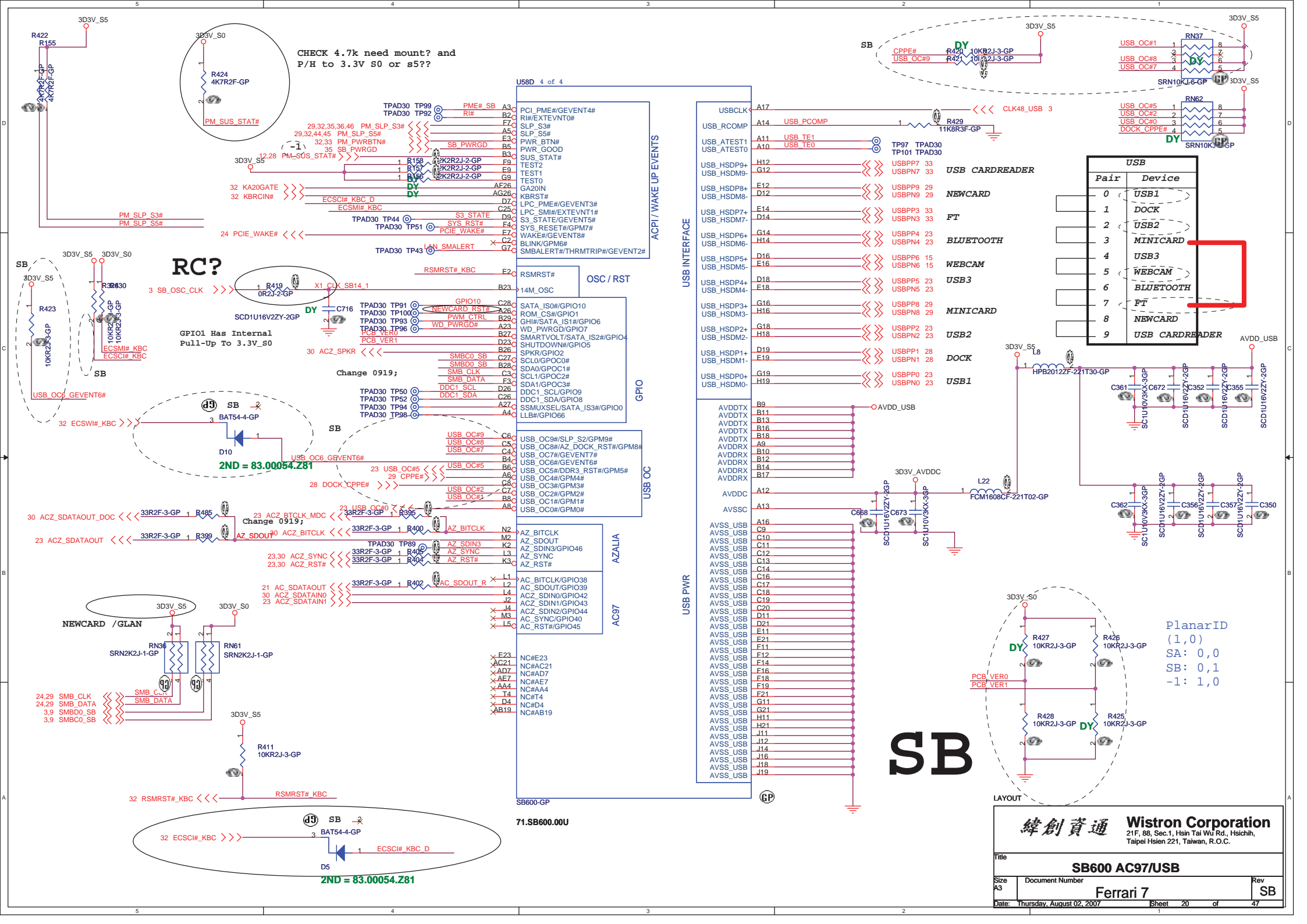
LAYOUT

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title SB600 ACPI/GPIO/SATA/IDE (2 of 5)  
Size A3 Document Number  
Date: Thursday, August 02, 2007 Sheet 18 of 47  
Ferrari 7 SB







CHECK 4.7k need mount? and P/H to 3.3V S0 or S5??

RC?

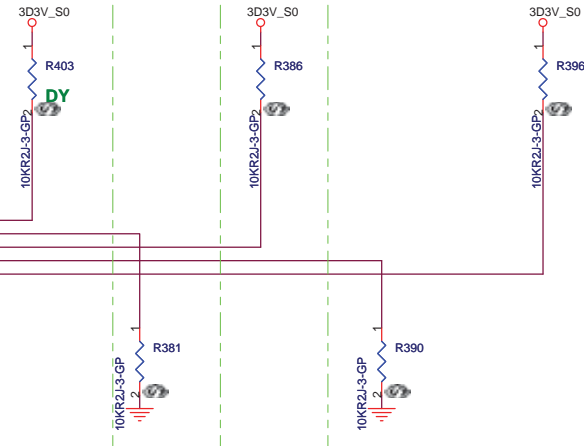
2ND = 83.00054.Z81

2ND = 83.00054.Z81

USB	
Pair	Device
0	USB1
1	DOCK
2	USB2
3	MINICARD
4	USB3
5	WEBCAM
6	BLUETOOTH
7	FT
8	NEWCARD
9	USB CARDREADER

PCI\_CLK4  
PCI\_CLK6  
PCI\_CLK0  
PCI\_CLK1

20 AC\_SDATAOUT  
17,32 PCLK\_KBC  
17 CLK33 LPCROM  
17,28 PCI\_CLK0  
17,26 PCLK\_PCM



REQUIRED SYSTEM STRAPS

SB600					
	AC_SDOOUT	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4	DEFAULT	

SB600 HAS 15K INTERNAL PU FOR PCI\_AD[23..28]

DEBUG STRAPS

	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH	RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT
STRAP LOW				USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE

LAYOUT

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

SB600 STRAPPING PIN

Size A3

Document Number

Ferrari 7

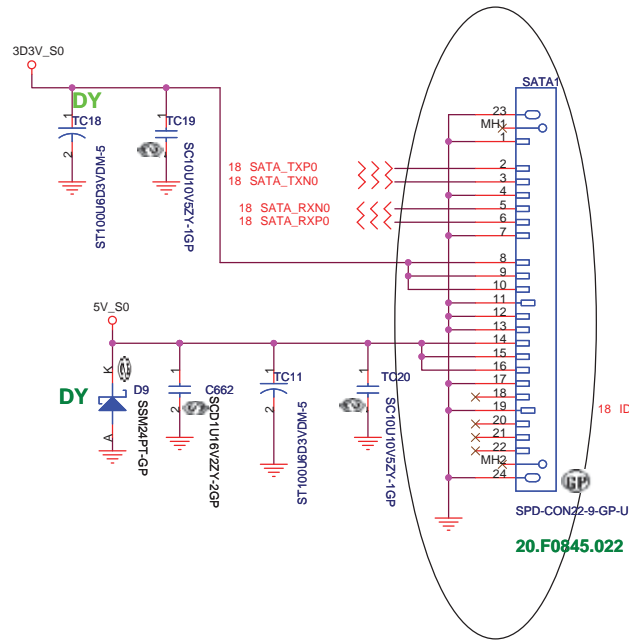
Rev SB

Date: Thursday, August 02, 2007

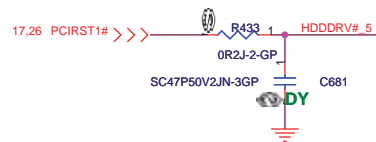
Sheet 21 of 47



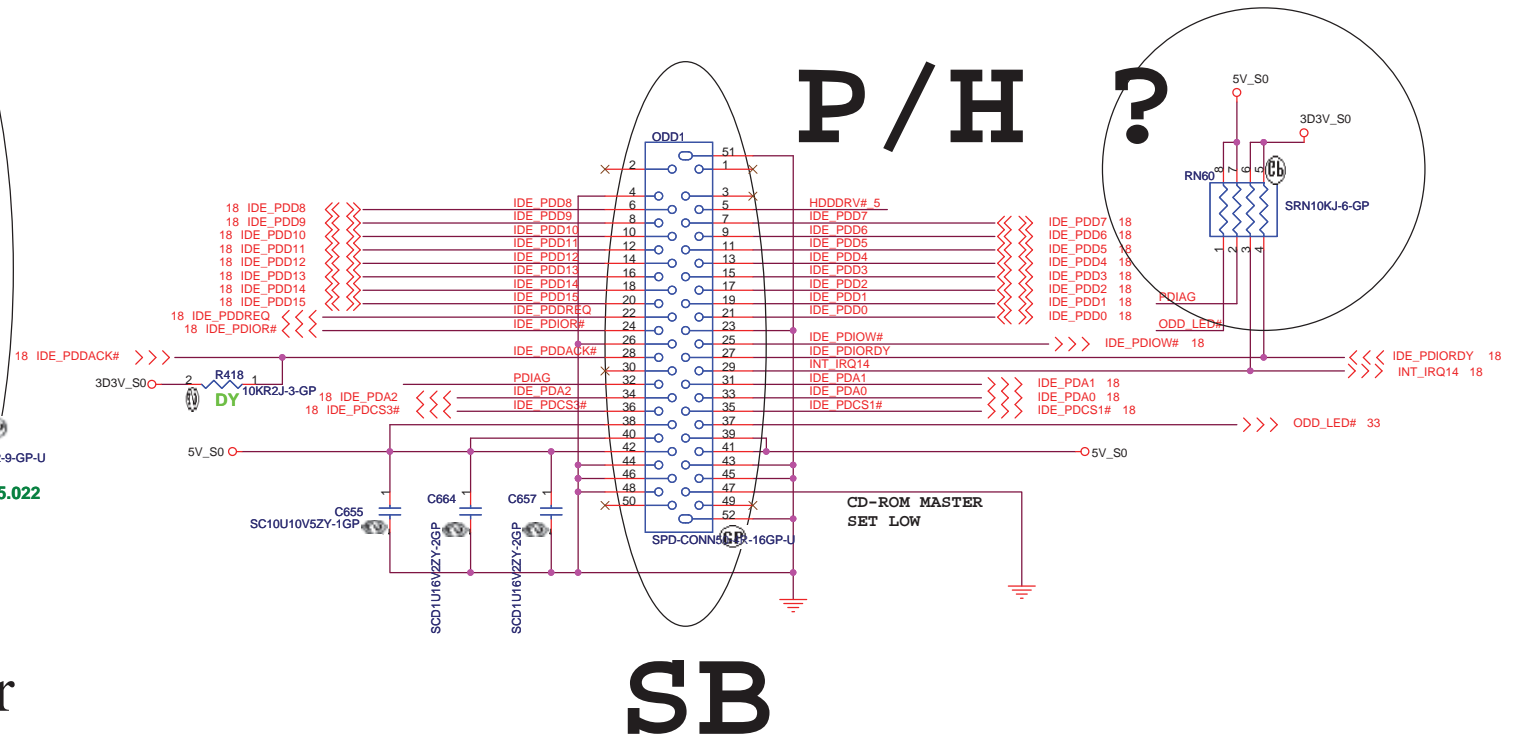
## SATA HD Connector



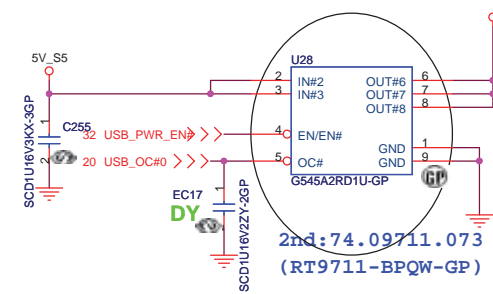
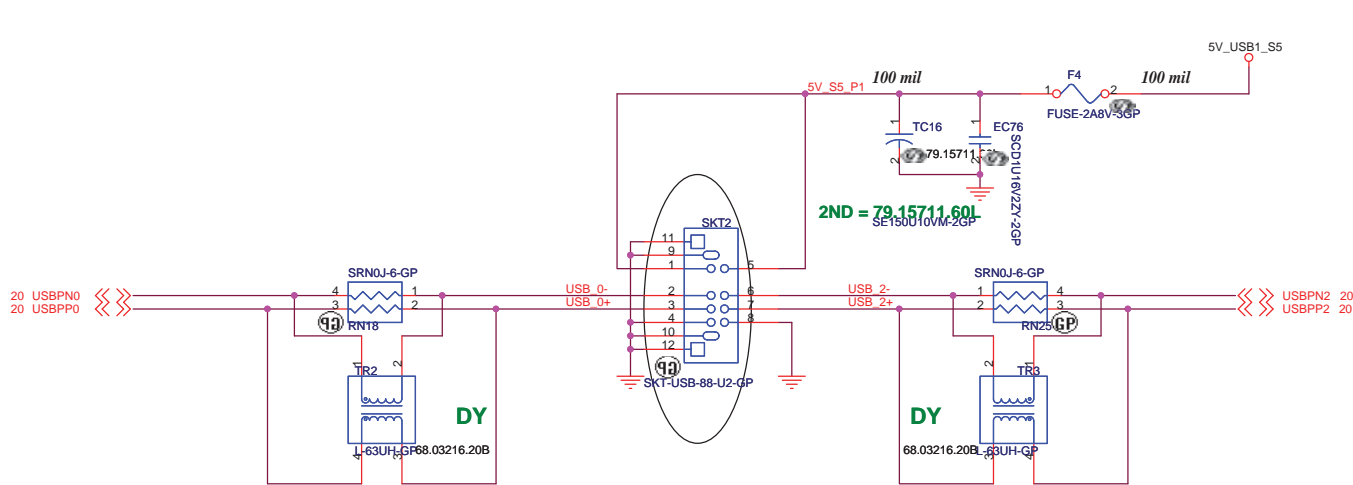
## HDD Connector



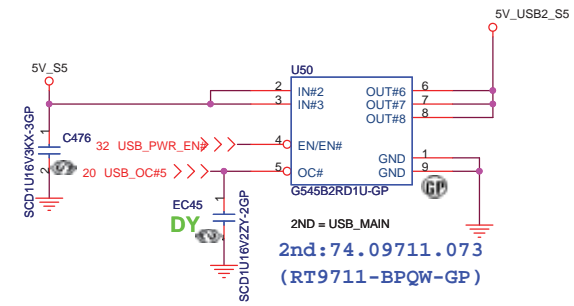
## CD-ROM Connector



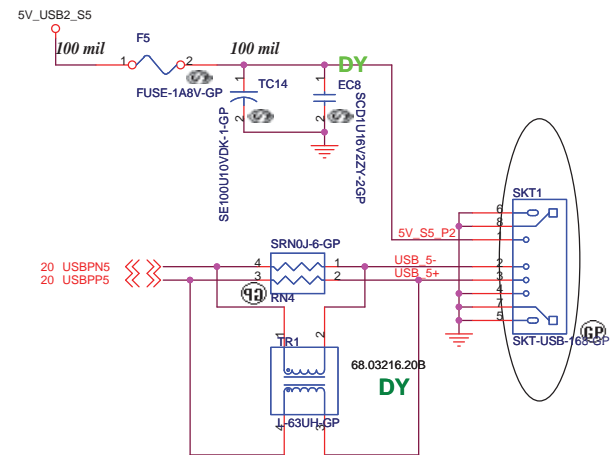




SB



2nd: 74.09711.073  
(RT9711-BPQW-GP)

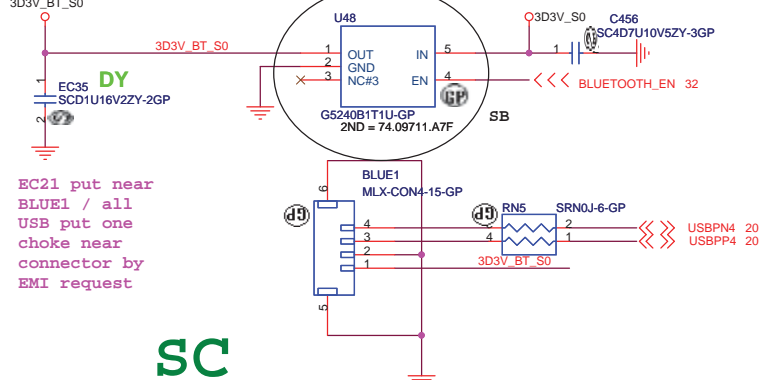


LAYOUT

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			
USB / MDC / BLUETOOTH			
Size	Document Number		Rev
	Ferrari 7		SB
Date:	Thursday, August 02, 2007	Sheet	23 of 47

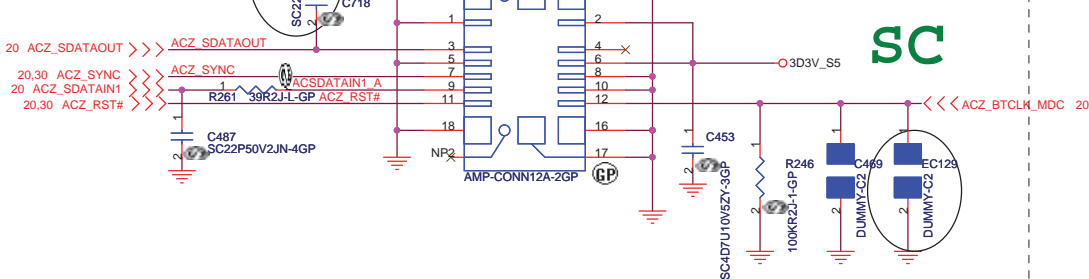
## BLUETOOTH MODULE



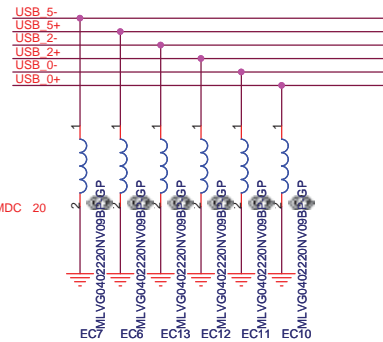
EC21 put near  
BLUE1 / all  
USB put one  
choke near  
connector by  
EMI request

SC

## MDC 1.5 CONN



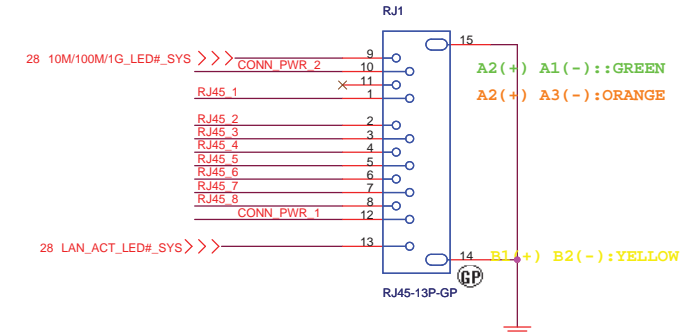
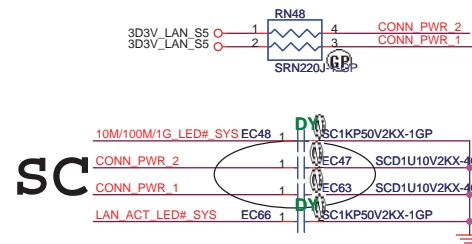
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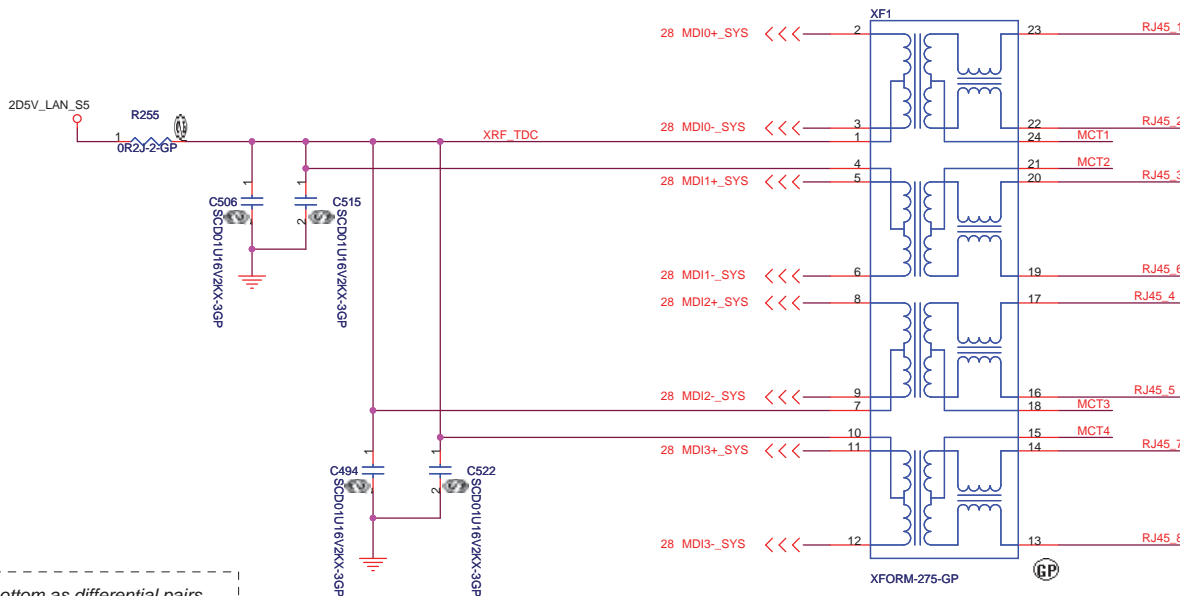
DY DY DY DY DY DY



# LAN Connector

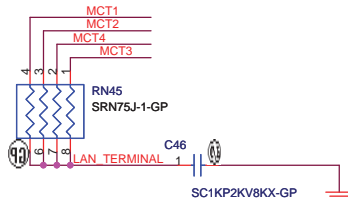


## GIGA Lan Transformer



- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

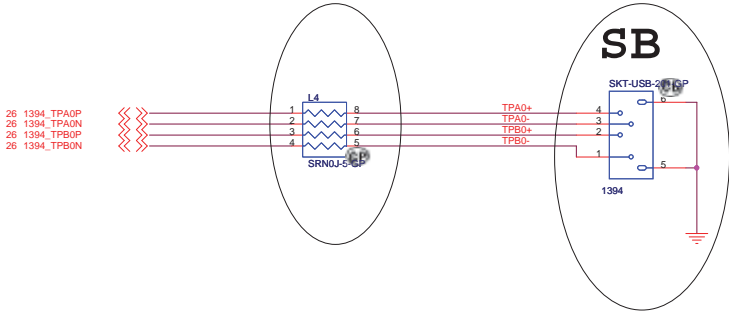


## LAYOUT

<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
<b>LAN Connector</b>		
Size A3	Document Number	Rev
<b>Ferrari 7</b>		<b>SB</b>
Date: Thursday, August 02, 2007	Sheet 25 of 47	

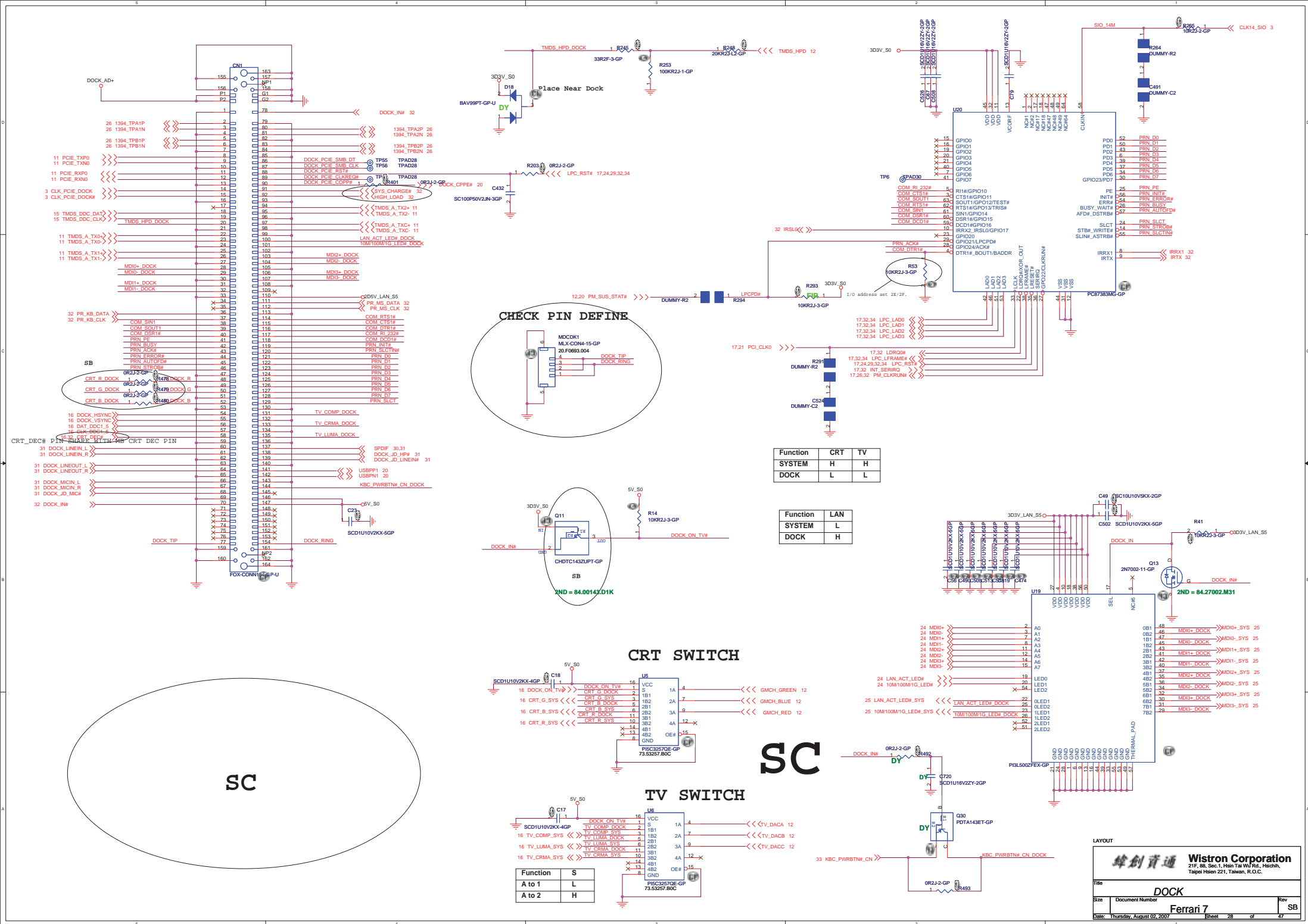


1394 Connector



LAYOUT

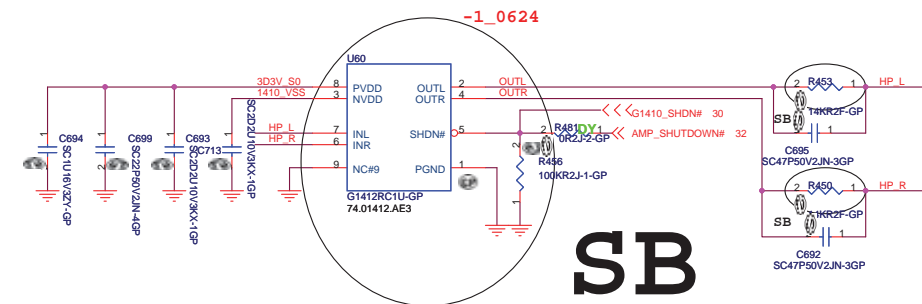
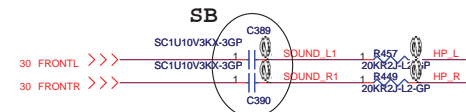
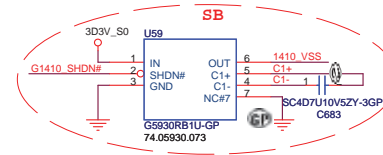
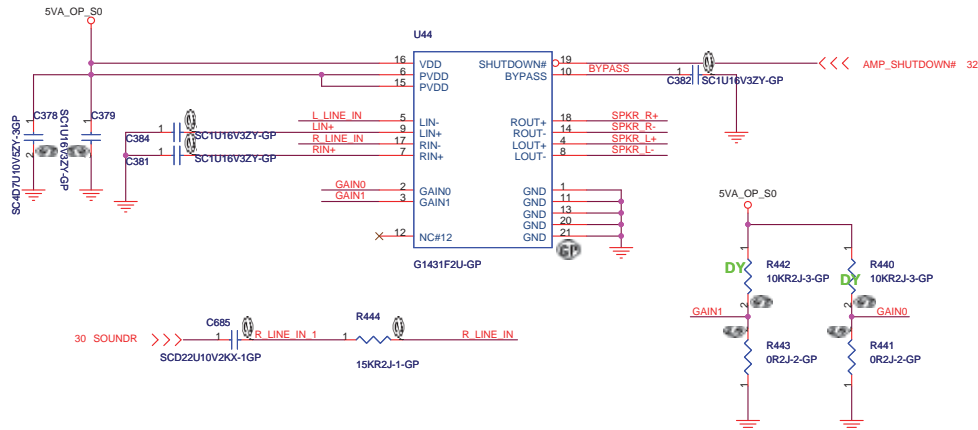
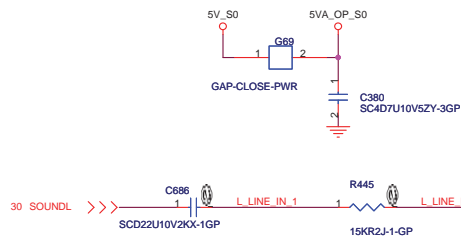
Title		Wistron Corporation	
Size		Document Number	
Date: Thursday, August 02, 2007		Sheet 27 of 47	
SB		Rev	
Ferrari 7		SB	



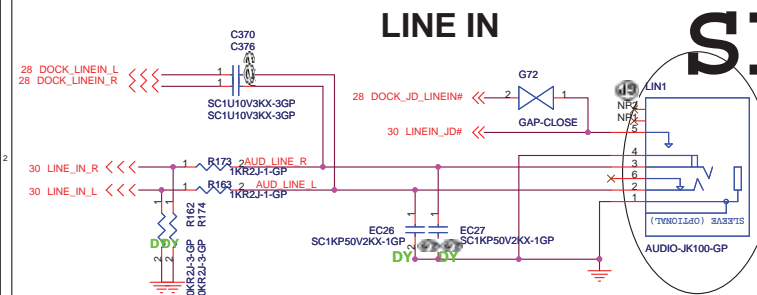




Date: Thursday, August 02, 2007 Sheet 30 of 47



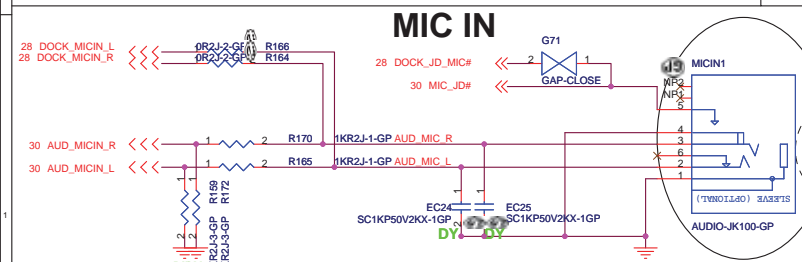
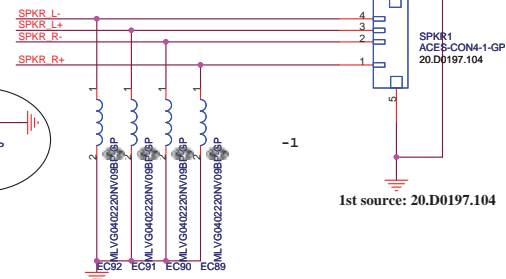
SB



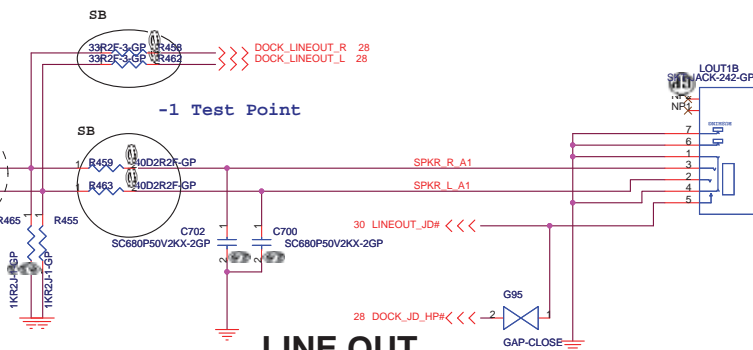
SB

SB

# Internal Speaker



SB

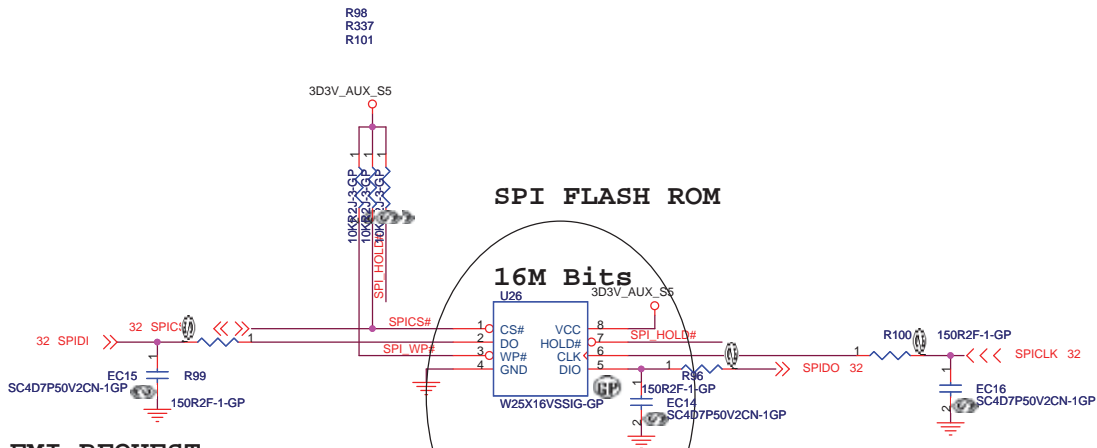


# LINE OUT

<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsin 221, Taiwan, R.O.C.		
Title	<b>AUDIO AMP AND JACK</b>	
Size	Document Number	Rev
	<b>Ferrari 7</b>	<b>SB</b>
Date: Thursday, August 02, 2007	Sheet 31	of 47

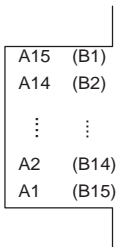






EMI REQUEST

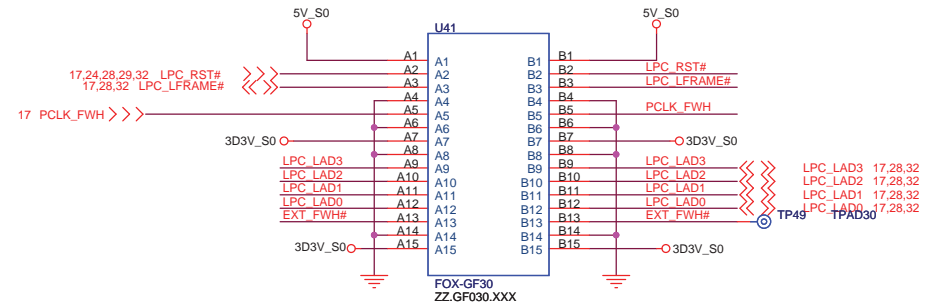
TOP VIEW



(BOTTOM VIEW)

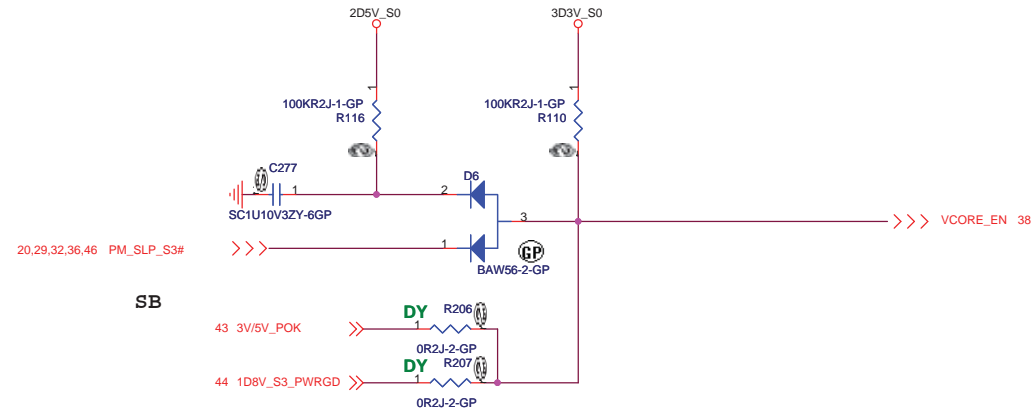
SB

GOLDEN FINGER FOR DEBUG BOARD

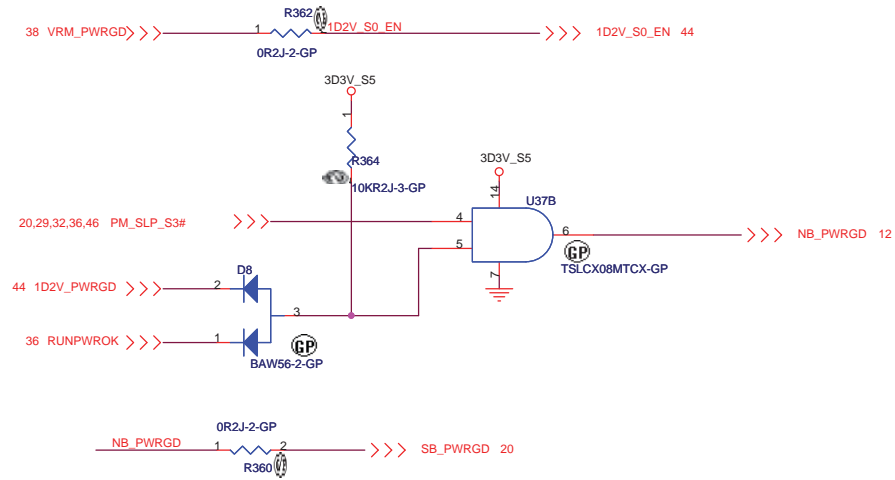


LAYOUT

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title BIOS		
Size A3	Document Number Ferrari 7	Rev SB
Date: Thursday, August 02, 2007	Sheet 34	of 47

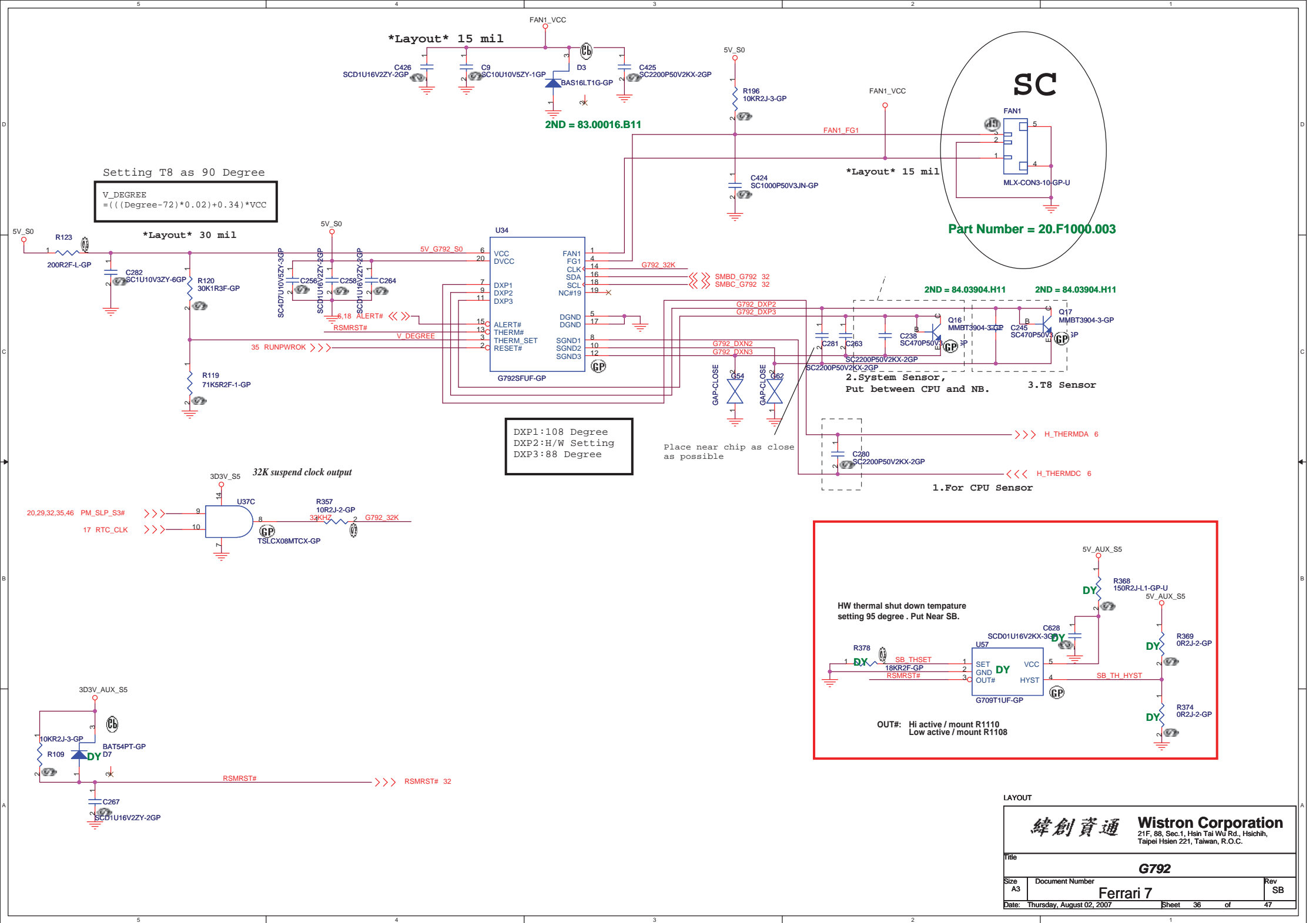


P/H @ 1D8V\_S3 PAGE

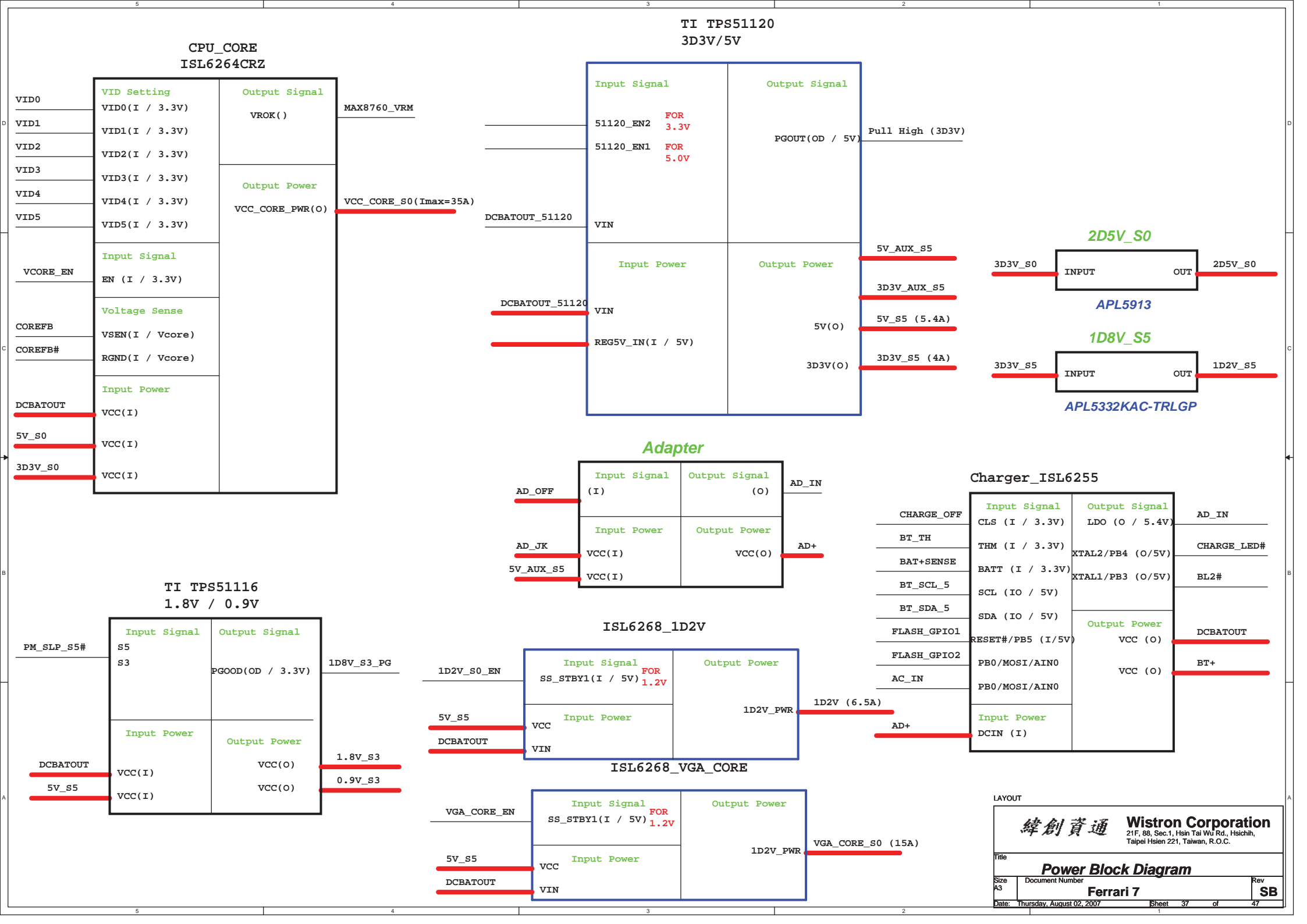


LAYOUT

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
POWERGOOD&ENABLES(1/2)			
Size	Document Number	Rev	
A3		SB	
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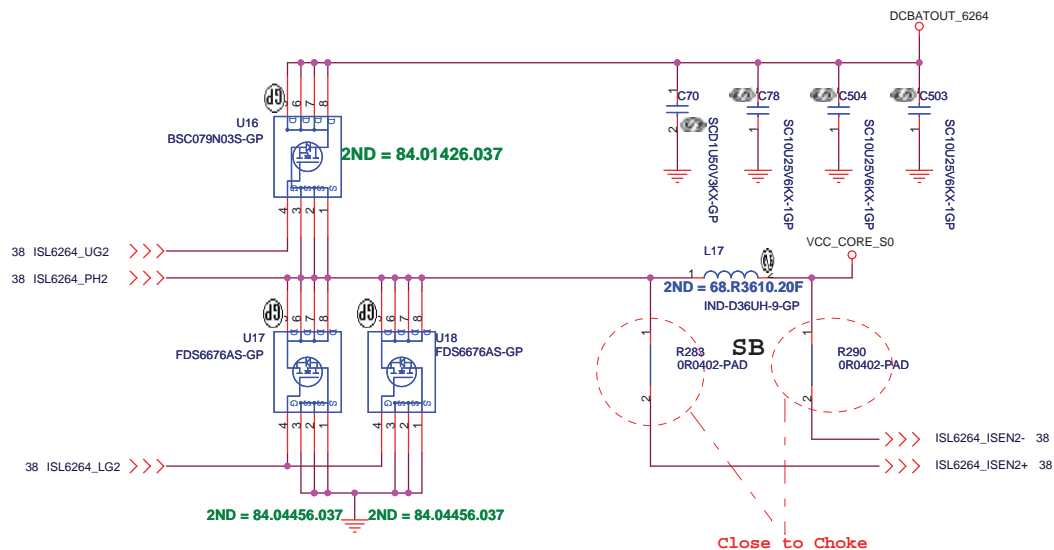
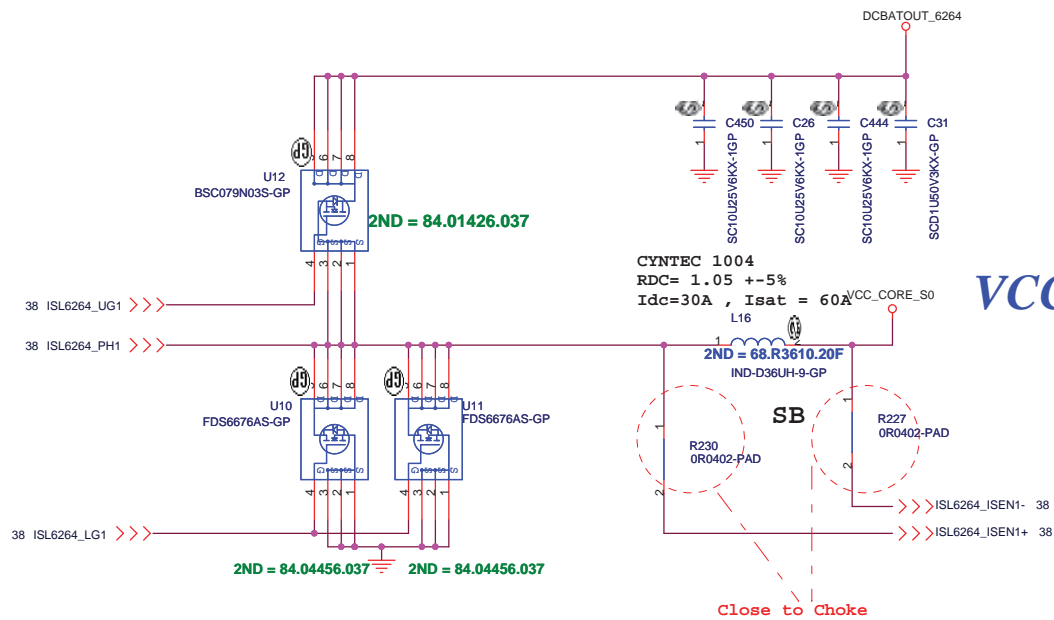




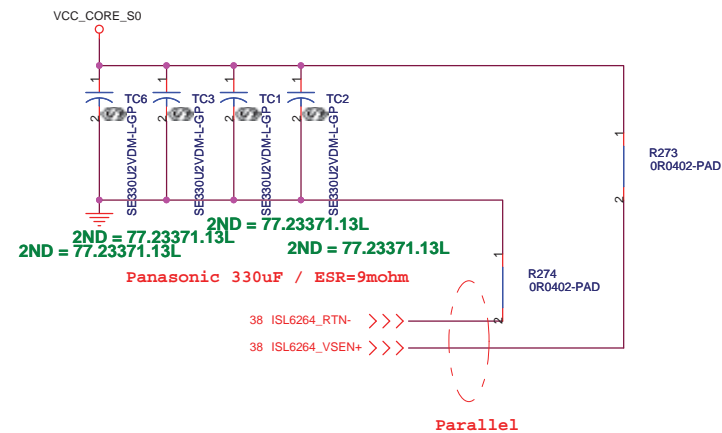
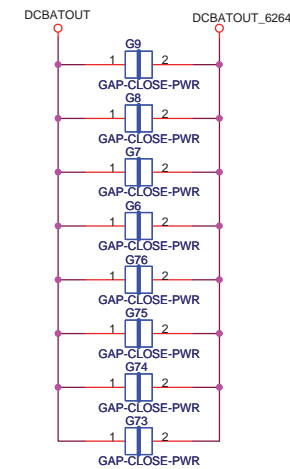


V1D5	V1D4	V1D3	V1D2	V1D1	V1D0	DAC
0	0	0	0	0	0	1.550
0	0	0	0	1	0	1.502
0	0	0	0	1	1	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	1	0	0	0	1.375
0	0	1	0	0	1	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	0	1	1	1	0.975
0	1	1	0	0	0	0.950
0	1	1	0	0	1	0.925
0	1	1	0	1	0	0.900
0	1	1	0	1	1	0.875
0	1	1	1	0	0	0.850
0	1	1	1	0	1	0.825
0	1	1	1	1	0	0.800
0	1	1	1	1	1	0.775
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.75
1	0	0	0	0	1	0.7375
1	0	0	0	1	0	0.725
1	0	0	0	1	1	0.7125
1	0	0	1	0	0	0.7
1	1	1	1	1	1	0.375





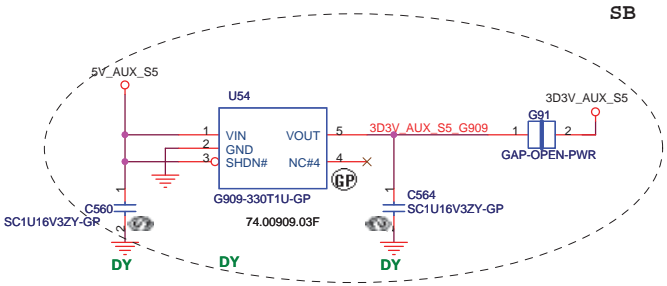
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LAYOUT

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Title			
<b>CPU Vcore Power_2</b>			
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Aux Power 3D3V\_AUX\_S5

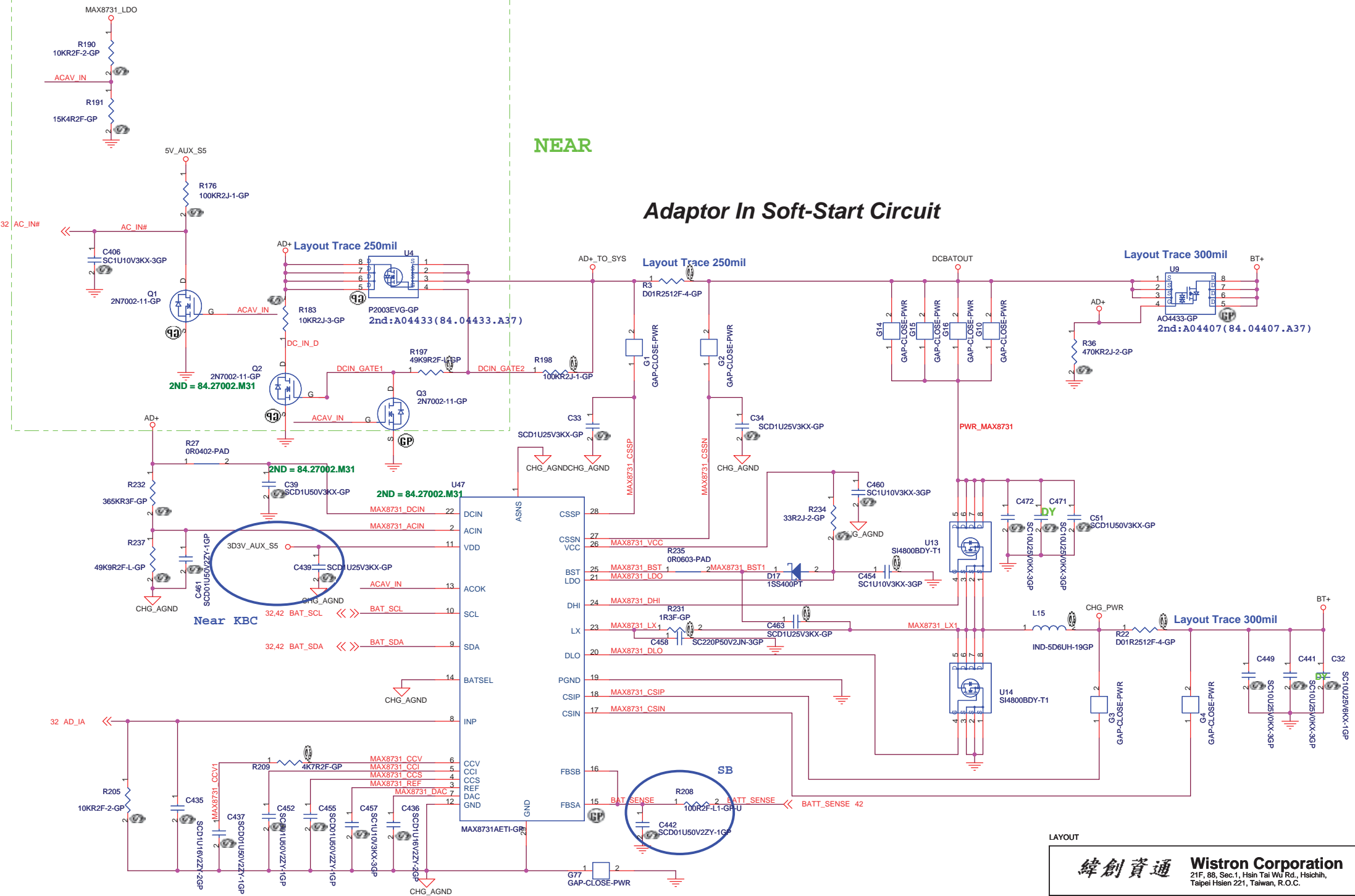


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<b>3D3V AUX</b>			
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NEAR

## Adaptor In Soft-Start Circuit

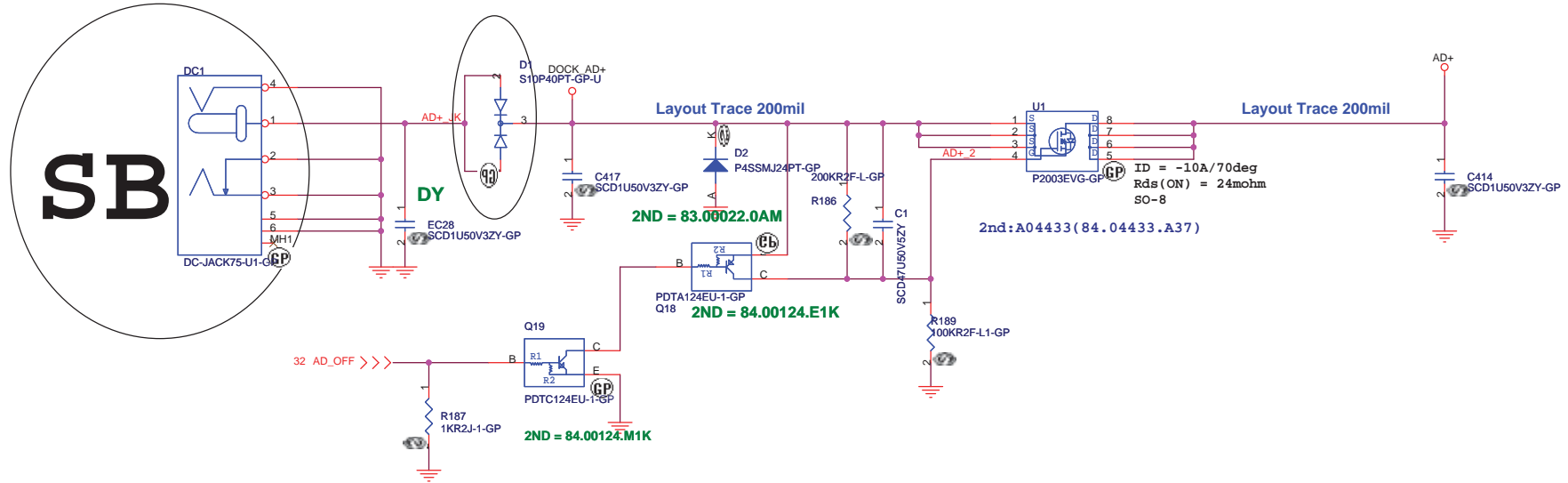


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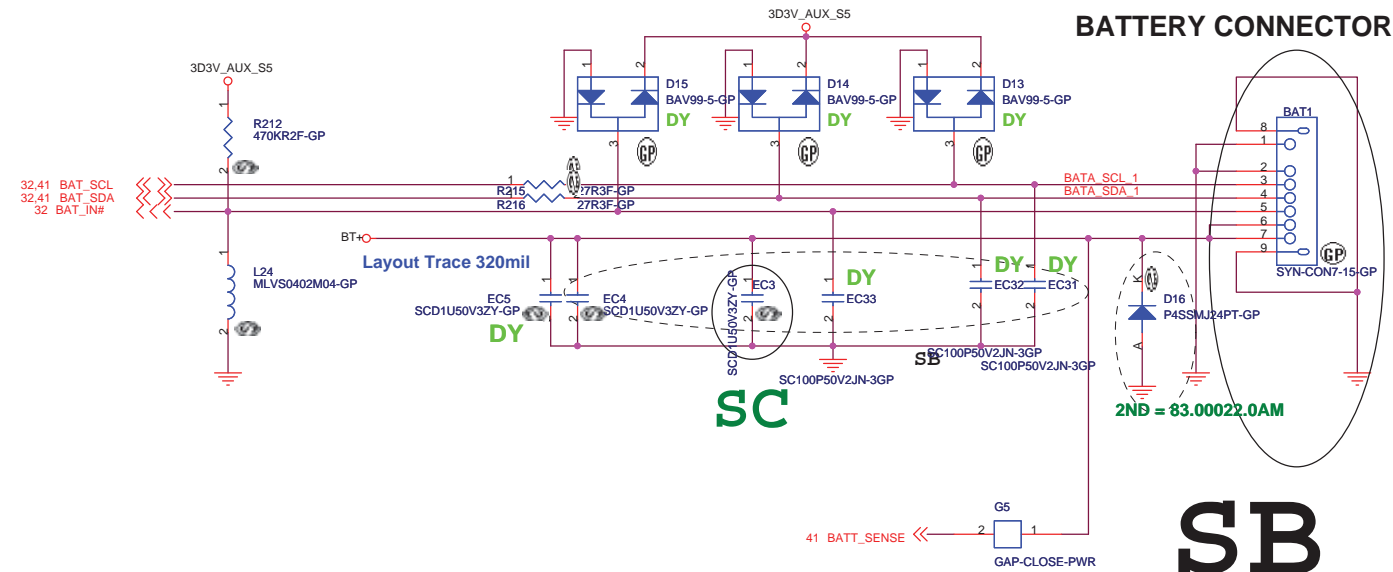
緯創資通 Wistron Corporation  
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CHARGER MAX8731			
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# Adaptor in to generate DCBATOUT



## BATTERY CONNECTOR



LAYOUT

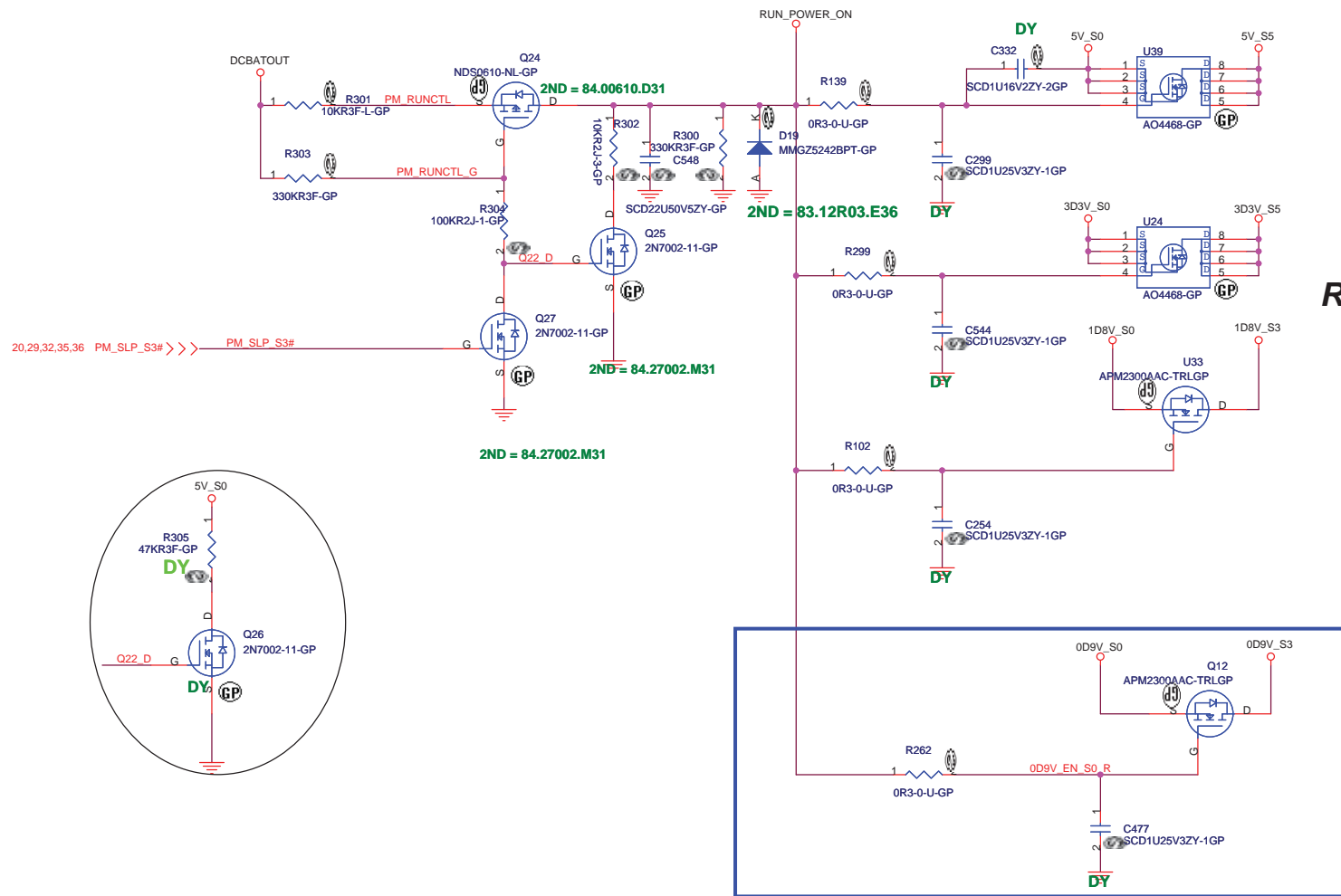
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>AD/BATT CONN</b>			
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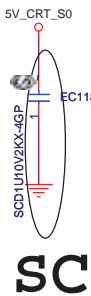
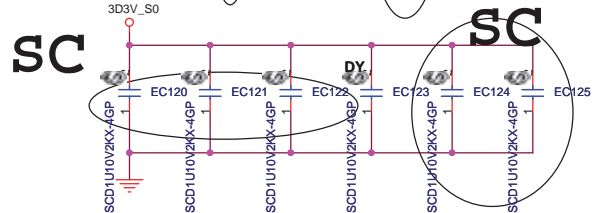
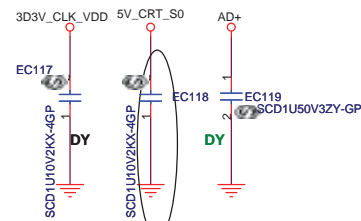
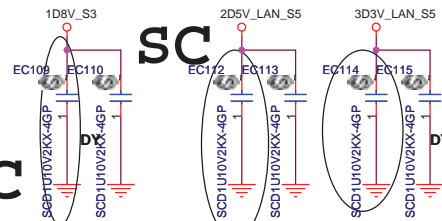
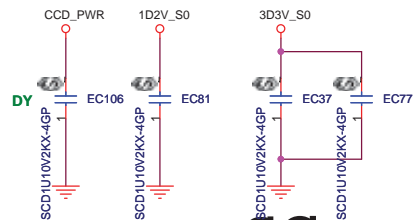
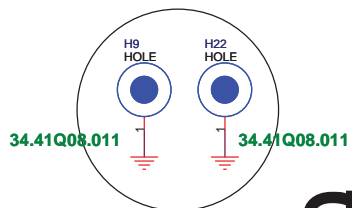
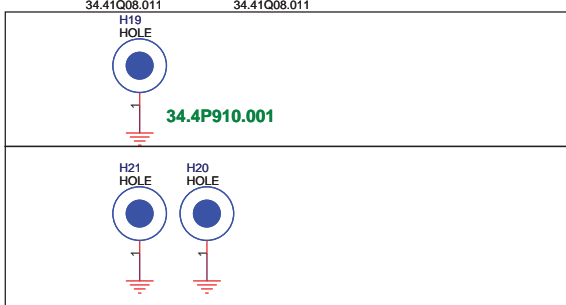
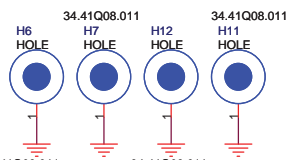
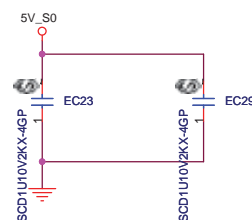
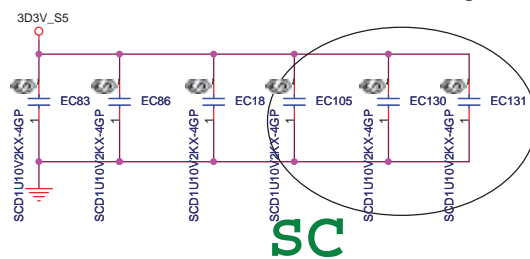
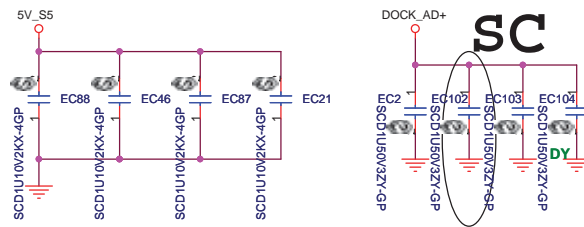
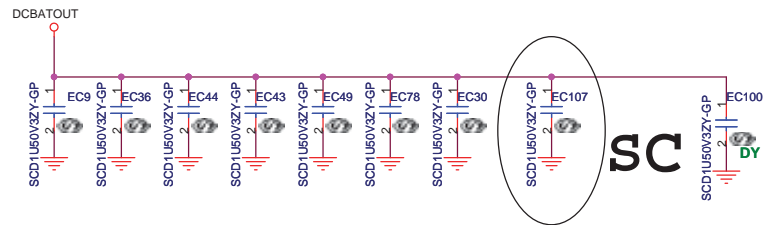
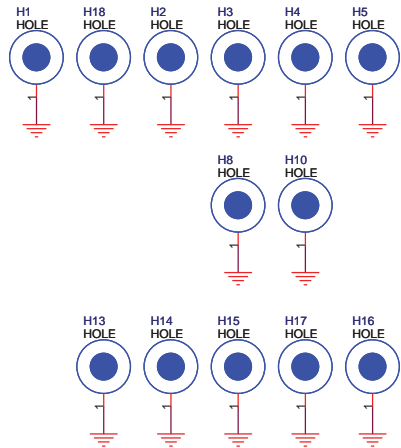






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<b>PWR CTL LOGIC / PWR PLANE</b>			
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